RELIABILITY REPORT 0409

35AMPS SINGLE PHASE BRIDGE IN GBPC PACKAGE

QUALIFICATION REPORT

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Section

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1. Introduction and Purpose:

The purpose of this qualification program is to qualify the **35Amps single-phase bridge assembled in GBPC package**. The test vehicles are GBPC3512A.
The data and report are generated by IRINDIA Reliability Laboratory.

2. Issue:

The results collected in this report are sufficient to release a Qualification Test results for the **35Amps single-phase bridge in GBPC package.**
The Qualification is justified by environmental testing, presented in this report, which ensures that the product under consideration fulfils the Market requirement and IRINDIA 's reliability requirements.
The Final Qualification is released for

35Amps Single Phase Bridge assembled in GBPC package.

3. Process Description:

The product family under consideration are assembled & processed at IRINDIA in standard manufacturing process.

4. Executive Summary:

Environmental testing for HTRB, TC, Moisture (85/85) & PC was performed on 4 lots
The lot was assembled in GBPC3512A.
Environmental testing included:

High Temperature Blocking Life Test (HTRB)
Temperature Cycling Test (TC)
Humidity Test (85 / 85)
Power Cycling Test (PC)

5. Environmental Stress Test Plan:

Part Number	Stress	Test Conditions	Sample Size/Lot	Lots No	Read-out Intervals
GBPC3512A	HTRB	960V @ 125^0 C, 1000 Hrs	10	4	0, 168, 500, 1000 hours
GBPC3512A	TC	-55^0C / $+150^0$C, 200 Cycles	10	4	0, 50, 100, 200 cycles
GBPC3512A	85 / 85	85^0C, 85% RH, 1000 Hrs	10	4	0, 168,500, 1000 hours
GBPC3512A	PC	$\Delta Tj = 80^0$C, 2000 Cycles	8	4	0, 500, 1000, 2000 cycles

6. Criteria for qualification:

Devices are expected to perform with maximum one failure on these stresses.

7. Summary of Environmental Stress Test Results:

7.1 High Temperature Blocking Life Test (HTRB)

7.1 HIGH TEMP. BLOCKING LIFE TEST (HTRB)

Test conditions: Voltage = 960 Vpk
Tc(max) = +125°C

Test Completed after 1000 Hours

Measured parameter	**Failure Criteria**
Irr @ $V_{rr\,max}$, T_{amb}	Irr increase more than 400% versus initial values
V_F @ $I_{F\,max}$, T_{amb}	UBL

Part Number	Assy Lot #	Sample Size	No. of Test Failures @ hours				Total Devices Failed
			0	168	500	1000	
GBPC3512A	LOT 1	10	0	0	0	0	**0**
GBPC3512A	LOT 2	10	0	0	0	0	**0**
GBPC3512A	LOT 3	10	0	0	0	0	**0**
GBPC3512A	LOT 4	10	0	0	0	0	**0**

7.2 Temperature Cycling Test (T/C)

7.2 TEMPERATURE CYCLING (T/C)

Test conditions: Tc(min)= -55 °C
Tc(max)= +150 °C
30 minutes at each temperature extreme

Test Completed after 200 Cycles

Measured parameter	**Failure Criteria**
V_F @ $I_{F\,max}$, T_{amb}	V_F increase more than 10% versus initial values
Irr @ $V_{rr\,max}$, T_{amb}	UBL

Part Number	Assy. Lot #	Sample Size	No. of Test Failures @ cycles				Total Devices Failed
			0	50	100	200	
GBPC3512A	LOT 1	10	0	0	0	0	**0**
GBPC3512A	LOT 2	10	0	0	0	0	**0**
GBPC3512A	LOT 3	10	0	0	0	0	**0**
GBPC3512A	LOT 4	10	0	0	0	0	**0**

7.3 Moisture Resistance Test (85 / 85)

7.3 MOISTURE RESISTANCE TEST (85 / 85)

Test conditions: Tc = 85 °C, 85 % RH

Test Completed after 1000 Hours

Measured parameter	**Failure Criteria**
Irr @ $V_{rr\,max}$, T_{amb}	Irr increase more than 400% versus initial values
V_F @ $I_{F\,max}$, T_{amb}	UBL

Part Number	Assy. Lot #	Sample Size	No. of Test Failures @ hours				Total Devices Failed
			0	168	500	1000	
GBPC3512A	LOT 1	10	0	0	0	0	**0**
GBPC3512A	LOT 2	10	0	0	0	0	**0**
GBPC3512A	LOT 3	10	0	0	0	0	**0**
GBPC3512A	LOT 4	10	0	0	0	0	**0**

7.4 Power Cycling Test (P/C)

7.4 POWER CYCLING TEST (P/C)

Test conditions: Temperature : Δ Tj = 80ºC

Cycle time : T_{ON} = 2 min , T_{OFF} = 6 min

Type of Cooling : Forced Air

I_{AV} = 18 A per leg

Test Completed after 2000 cycles

Measured parameter	**Failure Criteria**
V_F @ $I_{F\,max}$, T_{amb}	V_F increase more than 10% versus initial values
Irr @ $V_{rr\,max}$, T_{amb}	UBL

Part Number	Assy. Lot	Sample Size	No. of Test Failures @ cycles				Total Devices Failed
			0	500	1000	2000	
GBPC3512A	LOT 1	8	0	0	0	0	**0**
GBPC3512A	LOT 2	8	0	0	0	0	**0**
GBPC3512A	LOT 3	8	0	0	0	0	**0**
GBPC3512A	LOT 4	8	0	0	0	0	**0**

8.1 HIGH TEMPERATURE REVERSE BIAS (AC-HTRB)

Conditions:

Temperature T_j = 125°C.
Bias V_{RR} = 960 V_{pk}
Duration 1000 hours

Purpose.

The purpose of HTRB is to stress the device with applied bias in the blocking mode while at elevated junction temperature.
This will accelerate any blocking voltage degradation process.

Failure modes.

The primary failure mode for HTRB stress is a gradual degradation of the breakdown characteristics. It is related to the presence of foreign materials and polar ionic contaminants. These materials, migrating under application of electric field at high temperature, can perturb the electric field termination structure.

Sensitive parameters: I_{RR} @ V_{RRM}

Test Conditions.

At the HTRB Blocking Life Test the devices to be tested are mounted on hot plates. The temperature of the housings is adjusted such as to allow a temperature at the blocking junction at T = T_j(max), taking into account the blocking losses and the thermal characteristics of the DUT's. An AC voltage is applied which is 100 % of the indicated periodic allowable peak blocking voltage V_{RRM}. During the test, the temperature of the housing, the bias voltage and the leakage currents are monitored and recorded. The evaluation is done until end test time.

8.2 TEMPERATURE CYCLING

Conditions:	Temperature	Tc(min)= -55 °C ; Tc(max.)= +150 °C
	Time at each temperature	t = 30'
	Test Length	200 Cycles
	Bias	No Bias

Purpose:
The purpose of temperature cycling is to simulate thermal stresses that devices encounter in the actual circuit applications in combination with potentially extreme operating ambient temperatures. Some equipment is designed to be used in extreme environments, and subjected to daily temperature cycles.

Failure mode:
The primary failure mode for temperature cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue results from thermo mechanical stresses due to heating and cooling and will cause electrical or thermal performance to degrade.
If the degradation occurs at the solder/die interfaces, then the thermal resistance and the on resistance will slowly increase or become unstable with time.
The mechanical stresses can propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of an increase in the reverse leakage or degraded breakdown characteristics.

Sensitive parameters: I_{RR} @ V_{RRM}, V_F

Test Conditions.
At the Temperature Cycling Test the devices are kept into the 2 chambers having a high temperature chamber (+150 °C) and a low temperature chamber (-55 °C) for 30 minutes each.

8.3 MOISTURE RESISTANCE (85 / 85)

Conditions:	Temperature	Tc = 85 °C
	Humidity	RH = 85%
	Test Length	1000 Hours
	Bias	No Bias

Purpose:
The purpose of moisture resistance testing is to subject non-hermetic encapsulated devices to temperature and humidity extremes. This test is a method of examining the ability of a non-hermetic package to withstand the deterious effects of a humid environment. The devices are placed in a temperature and humidity chamber at ambient pressure.

Failure mode:
The following failure mode has been observed:
The ingression of water molecules into the active area on the surface of the die. Once sufficient water has accumulated in the region of electric field termination structure on the dice, the perturbation of that field begins to degrade the breakdown characteristics of the device.

Sensitive parameters: I_{RR} @ V_{RRM}, V_F

Test Conditions.
At the Moisture Resistance Test the devices are kept in chamber having a temperature (+85 °C) and humidity (85%RH) for the test duration.

8.4 POWER CYCLING

Conditions: Temperature : Δ Tj = 80ºC

Cycle time : T_{ON} = 2 min , T_{OFF} = 6 min

I_{AV} = 18 A per leg

Test Duration 2000 cycles

Purpose:

The purpose of power cycling is to simulate thermal and current pulsing stresses that devices encounter in the actual circuit applications when either the equipment is turned on and off or the power is applied to the device in short bursts interspersed with quiescent, low power periods.

Failure mode:

The primary failure mode for power cycling is a thermal fatigue of the silicon/metal interfaces and metal/metal interfaces. The fatigue results from thermo - mechanical stresses due to heating and cooling and will cause electrical or thermal performance to degrade.

If the degradation occurs at the solder/die interfaces, then the thermal impedance and the on resistance will slowly increase or become unstable with time.

The mechanical stresses from the application of power can also propagate fractures in the silicon when the die is thermally mismatched to the solder/heat sink system. These fractures will manifest themselves in the form of an increase in the reverse leakage or degraded breakdown characteristics.

Sensitive parameters: I_{RR} @ V_{RRM}, V_F