

Application Note

*i*MOTION™

Plug N Drive™ Application Overview

Integrated Power Module for Appliance Motor Drive

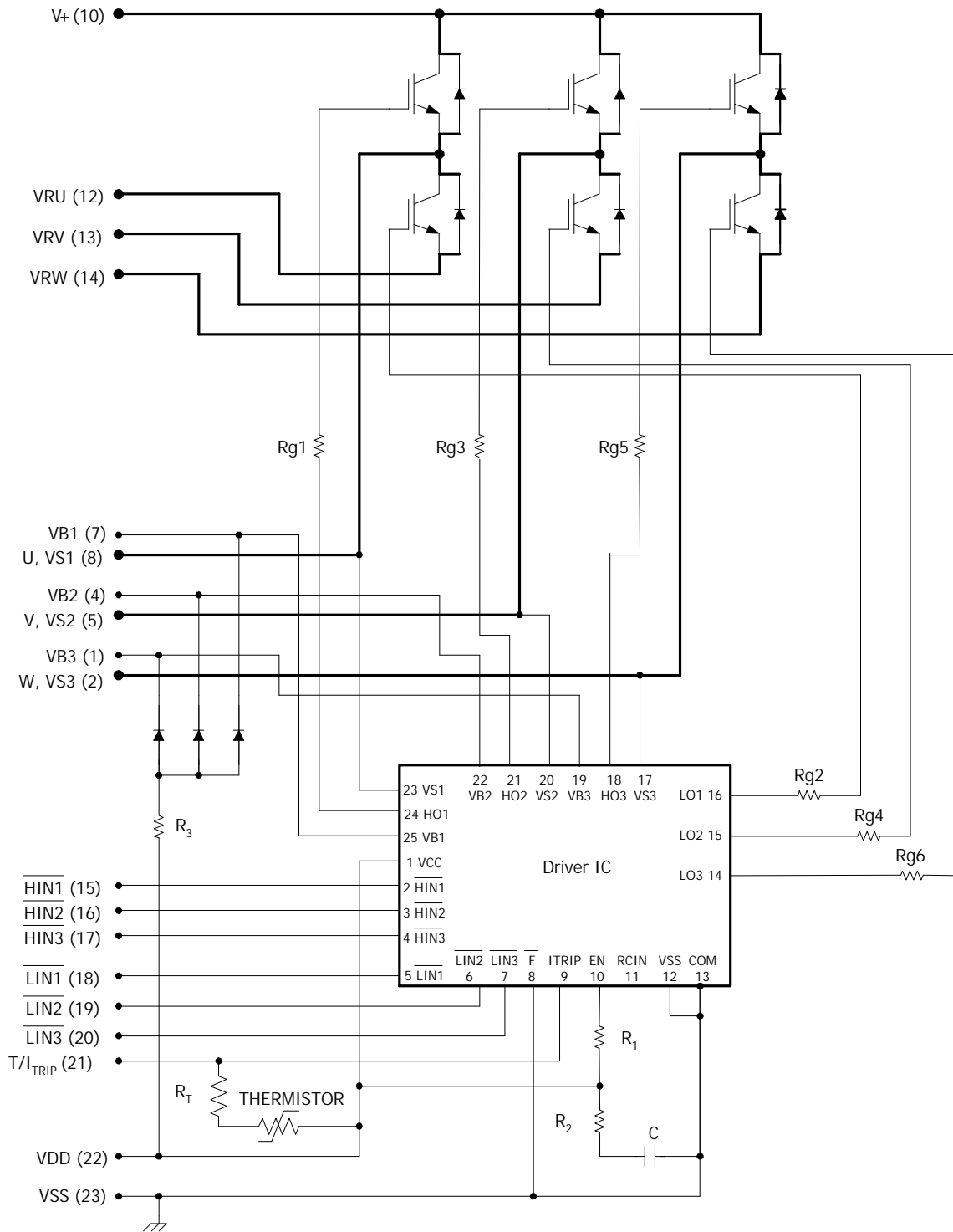
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Introduction

These modules represent a sophisticated, integrated solution for 3 phase motor drives used in a variety of appliances, such as washing machines, energy efficient refrigerators and air conditioning compressor drives in the 250 Watt to 2 Kilowatt power range. They utilize NPT(non-punch through) IGBTs matched with Ultra-soft recovery diodes to minimize EMI generation. In addition to the IGBT power switches, the modules contain a 6 output monolithic driver chip, matched to the IGBTs to generate the most efficient power switch consistent with minimum noise generation and maximum ruggedness.

- Packaging options include staggered pinout for maximum creepage distances and straight or 90° bend options for heat-sinks parallel or perpendicular to the circuit board.
- Capacitive switch noise coupling to the mounting surface is prevented by a ground plane isolated to 2000Vrms connected to the Vss pin.
- Insulated Metal Substrate technology ensures low thermal resistance and less stringent flatness requirements for the heat-sink. It also offers significant flexibility in the module layout and internal electrical system.



Plug N Drive™ Solution

Apart from the better known advantages of modules (smaller, more reliable, single component) compared with discrete solutions, the Plug N Drive modules relieve the designer from several pitfalls often associated with IGBT inverter designs:

- Lower circuit inductance than discrete solutions results in voltage spike reduction and the ability to operate at higher switching frequency with lower switch losses.
- Simple power connection, just V+, the emitter connections Le1, Le2 and Le3 and the motor connections U, V and W.
- The integrated driver requires only 6 logic level inputs. (includes 3.3V logic) and 3 bootstrap capacitors selected for the switching frequency.
- Propagation delays for all low-side and high-side IGBTs are matched to prevent DC core flux from being applied to the motor.
- Built in dead time control prevents conduction overlap between high-side and low-side IGBTs.
- Fail-safe operation is ensured by built in shut down features for over current and over temperature.
- Analog temperature monitor and phase leg current pins are provided.

Plug N Drive™ System Description

The primary advantage in using the Plug N Drive modules is the ease in which an optimized, reliable motor drive system can be implemented. The designer is relieved of the following headaches:

- How to provide sufficient dead time to prevent shoot through failures.
- How to design an overcurrent protection circuit to protect the IGBT switches.
- How to design an over-temperature detection circuit that actually monitors IGBT temperature.
- How to match propagation delay times in the drive circuits to prevent DC current flow in the motor windings.
- How to select the optimum switch times to minimize EMI generation and maximize efficiency.
- How to minimize inductive loop size for minimum turn-off voltage overshoots in the IGBTs.

The IRAMS module provides answers to all the above questions in a compact, electrically isolated package.

Internal circuitry

The 600V IRAMS module contains six IGBT die each with its own discrete gate resistor, six commutation diode die, one three phase monolithic, level shifting driver chip, three bootstrap diodes with current limiting resistor and an NTC thermistor/resistor pair for over temperature trip. The over current trip circuit responds to an input voltage generated from an external sense element such as a current transformer or sense resistor. The input pin for the trip circuit performs a dual function:

- Input pin for over current trip voltage.
- Output pin for module analog temperature sensing thermistor.

Because of the dual function requirements, an external circuit similar to the diagram below is recommended.

It is important that the Vcc filter capacitor is connected directly at the IRAMS module to prevent noise from propagating into the Itrip circuit to cause false tripping. The open collector, over current control transistor is normally 'on' and inhibits the over current function. The over temperature circuit is always active and is over-ridden by the current circuit in the event of over current detection.

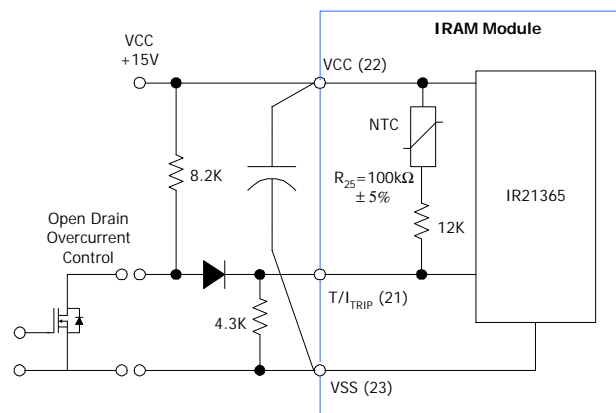


Figure 1: Over current interface circuit

Input signals

The complete, open loop motor drive system comprises a signal source, a drive stage and a power stage. The three phase motor can be a simple induction type, or a permanent magnet synchronous type. The IRAMS module integrates the driver and power stages into an isolated module but the 'brains' of the system must generate timing, speed and direction PWM or PFM information to complete the motor drive function.

5 volt logic systems are generally preferred from a noise

immunity standpoint but the module can also accept 3.3V logic or any pulse input up to the Vcc level (+15V).

The monolithic driver IC inputs require a logic low to command an output. The Itrip input is 4.3V nominal and the under voltage lockout voltage is 11V. Further information on IR21365 characteristics is available at www.irf.com.

IRAMS10UP60A Pin Description

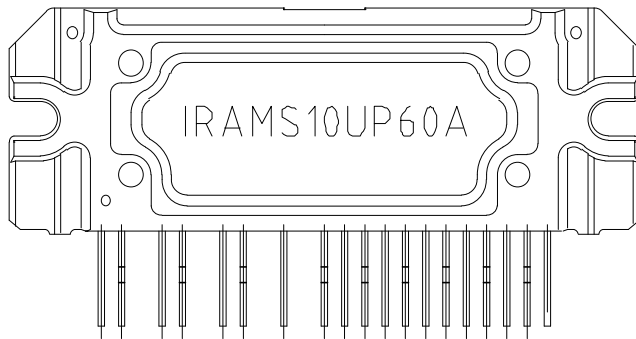


Figure 2: Power module PIN out.

Pin	Label	Description
1:	VB3	Bootstrap capacitor Phase W.
2:	VS3	Phase W output (high-side emitter Phase W)
3:		Position empty for creepage voltage.
4:	VB2	Bootstrap capacitor Phase V.
5:	VS2	Phase V output (high-side emitter Phase V)
6:		Position empty for creepage voltage.
7:	VB1	Bootstrap capacitor Phase U.
8:	VS1	Phase U output (high-side emitter Phase U)
9:		Position empty for creepage voltage.
10:	V+	Positive bus voltage.
11:		Position empty for creepage voltage.
12:	Le1	Low-side emitter Phase U.
13:	Le2	Low-side emitter Phase V.
14:	Le3	Low-side emitter Phase W.
15:	HIN1	High-side input Phase U.
16:	HIN2	High-side input Phase V.
17:	HIN3	High-side input Phase W.
18:	LIN1	Low-side input Phase U.
19:	LIN2	Low-side input Phase V.
20:	LIN3	Low-side input Phase W.
21:	ITRIP	Over current and temperature shut-down.

22: VCC

+15V bias voltage.

23: VSS

15V return and substrate ground plane.

Bootstrap Circuit Operation.

The high and low-side driver IC requires a floating voltage supply for each of the three high-side circuits that provide gate pulses to high-side IGBTs. A very convenient way of obtaining such floating voltage supplies is usage of bootstrap circuits. The following figure shows such an implementation for one phase of a three-phase switching inverter drive. The circuit is repeated for each phase.

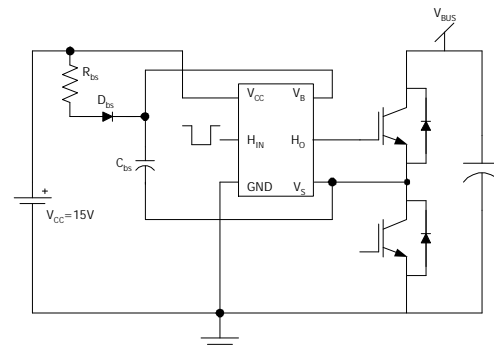


Figure 3: Schematic showing bootstrap circuit for one phase

Operation of the circuit is as follows

When the low-side IGBT is on, the bootstrap capacitor Cbs charges through the bootstrap diode Dbs, resistor Rbs and low side switch S2 to almost 15 V, since the Vs pin of the IC is almost at ground potential. The capacitor Cbs is so designed that it retains most of the charge when the low-side device switches off and the Vs pin goes to almost the bus potential. Then, the voltage Vbs being almost 15 V, the high-side circuit of the driver IC is biased by the capacitor Cbs. Selection of the bootstrap capacitor, diode and resistor is governed by several factors:

1. Voltage Vbs has to be maintained at a value higher than the under-voltage lockout level for the IC driver.
2. The capacitor Cbs does not charge exactly to 15V when the low-side switch is turned on, depending upon the drop across the bootstrap diode (V_{fbs}) and low-side switch (V_{ceonS2}).
3. When the high side switch is on, the capacitor discharges mainly via the following mechanisms:
 - a. Gate charge Q_g for turning the high-side switch on
 - b. Quiescent current I_{qbs} to the high-side circuit in the IC

- c. Level-shift charge Q_L s required by level-shifters in the IC
- d. Leakage current I_{DL} in the bootstrap diode D_{BS}
- e. Capacitor leakage current I_{CBS} (ignored for non-electrolytic capacitors)
- f. Bootstrap diode reverse recovery charge Q_{RRBS}

Charge lost by the bootstrap capacitor in one switching cycle is given by the following equation:

$$\Delta Q_{BS} = Q_G + Q_{RRBS} + \frac{I_{QBS}}{f_{sw}} + Q_{LS} + \frac{I_{DL}}{f_{sw}} \quad (1)$$

where f_{sw} is the switching frequency and the other parameters are as defined earlier. This charge loss in the bootstrap capacitor as given above results in a drop in the voltage V_{BS} across it. The value of C_{BS} can be designed based on the desired voltage drop in V_{BS} as follows,

$$C_{BS} = \frac{\Delta Q_{BS}}{\Delta V_{BS}} \quad (2)$$

The drop in V_{BS} can be set as a percentage of the value of V_{BS} before turn-on of the high side switch. The lowest value of V_{BS} in one modulation cycle is given by

$$V_{BS} = V_{CC} - V_{FBS} - V_{CEON(S2)} \quad (3)$$

Note that the above equation gives the worst-case value of the bootstrap voltage with the low side IGBT conducting current in conjunction with high side diode. Current reversal leads to low side diode conduction in conjunction with the high side IGBT, whereupon the equation (3) changes to:

$$V_{BS} = V_{CC} - V_{FBS} + V_{F(D2)} \quad (3a)$$

Combining equations (1), (2) and (3) and using $\Delta V_{BS} = 1\%$ of V_{BS} , we get:

$$C_{BS} = \frac{Q_G + Q_{RRBS} + \frac{I_{QBS}}{f_{sw}} + Q_{LS} + \frac{I_{DL}}{f_{sw}}}{0.01 \cdot (V_{CC} - V_{FBS} - V_{CEON(S2)})} \quad (4)$$

A series resistor R_{BS} is recommended as shown in figure 3. This limits peak currents in the bootstrap circuit during initial charging. These currents, if excessive, have been known to cause driver latch-up under fast switching conditions. Typically, the low side switch is switched with a constant duty-cycle for charging the bootstrap capacitor initially. The time required for the initial bootstrap capacitor charging, after which input signals can be transferred to the switch gates, is given by:

$$t \geq \frac{C_{BS} \cdot R_{BS}}{D} \cdot \ln \left(\frac{V_{CC}}{V_{CC} - V_{BS(\min)} - V_{FBS} - V_{CEON(S2)}} \right) \quad (5)$$

In the above equation, D is the duty cycle of the charging pulses. Note that this discounts effects of discharging pro-

cesses and hence gives a minimum charging time.

BOOTSTRAP DIODE

When high side switch or diode conducts, the bootstrap diode supports the entire bus voltage. Hence for a 300-400 V system, D_{BS} has to be rated at 600 V. The peak current seen by D_{BS} is determined by the series resistor R_{BS} . However since this current spike is quite narrow, it does not seriously affect diode selection. Average current handled by the bootstrap diode is given by the product of the charge supplied to C_{BS} during every switching cycle expressed by equation (1) and the switching frequency f_{sw} . In order to minimize the power loss in the diode and to reduce the size of the bootstrap capacitor, reverse recovery charge in D_{BS} should be as low as possible. For the same reason, reverse leakage current should also be low at the highest operating temperature. Finally, the knee voltage of the diode should be low to minimize the voltage drop across it during charging.

LOW MODULATION FREQUENCY OPERATION

As was seen from equations (3) and (3a), the voltage across the low side device (IGBT or diode) reverses polarity with direction of current flow. Hence the voltage applied across the bootstrap circuit also varies accordingly, decreasing below V_{CC} when the low side IGBT conducts and increasing beyond V_{CC} when the low side diode conducts. This variation can be approximated for analysis to be sinusoidal in nature. For a sine current application the assumption is quite valid, since for practical current values, the voltage drop across the IGBT or diode varies almost linearly with current, except at very small current values. Then the voltage applied across the bootstrap circuit can be represented by:

$$V = V_{CC} - V_{PKI} \sin \omega t \quad (6)$$

when the low side IGBT is conducting with V_{PKI} representing peak voltage across the IGBT. Similarly, when the low side diode conducts, the equation above becomes:

$$V = V_{CC} + V_{PKD} \sin \omega t \quad (7)$$

where V_{PKD} represents the peak voltage across the low side diode. In the above equations (6) and (7), ω is the angular frequency corresponding to the modulation frequency f .

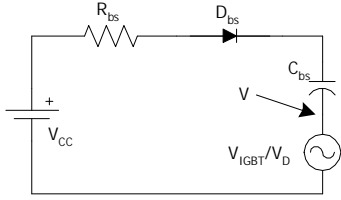


Figure 4: Schematic showing effect of low side switch/diode conduction

The above schematic represents the situation for a single phase of the three-phase inverter. This is briefly analyzed below:

When the modulation frequency is lower than the cutoff frequency for the bootstrap circuit defined by the resistor R_{bs} , bootstrap diode voltage drop V_{fbs} and the capacitor C_{bs} , the capacitor voltage varies with time at the modulation frequency. When the low side IGBT is conducting, applied voltage across the bootstrap circuit reduces sinusoidally, which means that the voltage across the sine voltage source in figure 4 is positive and increasing. Starting from the initial capacitor voltage of approximately V_{cc} , the bootstrap diode is reverse biased while the voltage V is rising from zero to V_{pk} . During each switching cycle, the voltage V changes by small value from the previous switching cycle by:

$$\Delta V = V_{PKI} [\sin \omega(t + T_{sw}) - \sin \omega t] \quad (8)$$

where T_{sw} is the switching period. In this time, the capacitor discharges because of I_{qbs} and I_{dl} only, since the high side IGBT is not switching. There is no charging of the bootstrap capacitor, the diode D_{bs} being reverse biased. Capacitor voltage therefore decreases approximately in a linear fashion. As the voltage V crosses V_{pk} , the capacitor voltage is already at a steady value given by the difference between V_{cc} and V_{pk} . After this, the voltage V decreases sinusoidally and the capacitor voltage follows the sine wave till the voltage V reaches zero. During this quarter cycle from V_{pk} to zero, the diode D_{bs} is forward biased enabling bootstrap capacitor charging. The charge supplied per cycle is then equal to the charge lost in the quiescent currents plus the charge required to raise the capacitor voltage by the change in V in one switching cycle, which is:

$$\Delta V = V_{PKI} [\sin \omega(t + T_{sw}) - \sin \omega t] \quad (9)$$

Thus the charge supplied per switching cycle is:

$$\Delta Q = CV_{PKI} [\sin \omega(t + T_{sw}) - \sin \omega t] + \frac{I_{QBS} + I_{DL}}{f_{sw}} + Q_{RRBS} \quad (10)$$

The term in brackets is approximately equal to the product of first differential of $\sin \omega t$ with respect to t , and the switching time T_{sw} . This has a maximum value of ωT_{sw} . Then the worst-case average current through the bootstrap circuit dur-

ing the quarter cycle under consideration is:

$$I_{AVG} = \left\{ CV_{PKI} \omega T_{sw} + \frac{I_{QBS} + I_{DL}}{f_{sw}} + Q_{RRBS} \right\} f_{sw} \quad (11)$$

When the voltage V crosses zero and becomes negative, the above analysis still applies with the additional charge required for switching the high side device. Then the worst-case average current in the bootstrap circuit is:

$$I_{AVG} = \left\{ CV_{PKD} \omega T_{sw} + \frac{I_{QBS} + I_{DL}}{f_{sw}} + Q_G + Q_{LC} + Q_{RRBS} \right\} f_{sw} \quad (12)$$

This continues for one quarter-cycle before the voltage V reaches V_{pk} . After V crosses V_{pk} and starts increasing to zero, the bootstrap diode is reverse biased and the capacitor discharges every cycle without a refresh charge. Hence the voltage across the capacitor goes on decreasing. Since the resistor R_{bs} carries bootstrap currents for all three phases, the worst case current for one quarter of the modulation period at a stretch (neglecting the 120° phase difference) is three times the value given in equation (12).

It is seen from equation (12) that the first term is independent of the switching frequency and depends upon the voltage drop across the low-side devices, the value of the bootstrap capacitor and the angular frequency corresponding to the sinusoidal modulation. The rest of the expression is the product of the refresh charge calculated in equation (1) and the switching frequency. This part is independent of the modulation frequency.

The IR module IRAMS10UP60 contains three bootstrap diodes and a series resistor connected internally between the 15 V supply V_{cc} and individual V_b pins of the three phases. Hence only appropriate bootstrap capacitors need be connected on the external board. Some layout aspects have to be considered before doing that. Bootstrap capacitors should be connected as close to the V_b and V_s pins as possible to reduce stray inductance in the connections. Furthermore, it is recommended to use a small high frequency capacitor in parallel to a larger low frequency bootstrap capacitor.

It can be shown that the power loss in the series resistor selected is well within limits. From equation (12), substituting under worst conditions:

$C = 10\mu F$, $V_{pk} = 2.5V$, $\omega = 2\pi \times 100\text{rad/s}$, $f_{sw} = 20\text{kHz}$, $I_{qbs} = 150\mu A$, $I_{dl} = 5\mu A$, $Q_g = 40\text{nC}$, $Q_{lc} = 5\text{nC}$, $Q_{rrbs} = 25\text{nC}$, we get $I_{AVG} = 17.3\text{ mA}$.

Then average resistor current = 50 mA

Using $I_{RMS} = 1.5 I_{AVG}$, $I_{RMS} = 75\text{ mA}$. This gives the resistor power loss 11.25 mW.

Note that this is under the absolute worst conditions assuming continuous current through the resistor and neglecting the phase difference between the bootstrap current components from the three phases.

POWER LOSS ESTIMATION

The IRAMS modules use 600 V non-punch-through (NPT) IGBTs with a 10 μs short-circuit capability, that are well optimized for switching and conduction losses. Hyperfast diodes with very low reverse recovery charge and reduced forward drop at high temperatures further improve the turn-on performance of the IGBTs. As the conduction losses are approximately constant with switching frequency for a given current and bus voltage levels, appropriate trade-off has to be obtained in selecting the switching frequency best suited for a particular device.

There have been many attempts to estimate switching energy values at turn-on and turn-off based on semiconductor device models. However the complexity associated with making such models accurate suggests that a more pragmatic approach would be measuring elemental energy losses and calculating total power losses using system level models. Switching losses for IGBT and diode can be measured and modeled empirically as functions of voltage, current and temperature. Similarly on-state voltage drop can be represented as a function of current and temperature.

$$\begin{aligned} E_{ON} &= (h1 + h2.I^x)I^k \\ E_{OFF} &= (m1 + m2.I^y)I^n \\ V_{CEON} &= V_T + aI^b \end{aligned} \quad (13)$$

In the above equations, V_T is the voltage drop across the IGBT/diode at zero current and $h1$, $h2$, x , k , $m1$, $m2$, y and n are empirical parameters obtained to get a good curve-fit between measured and calculated values. Then knowing the current variation with time and knowing the switching frequency, each of the above losses can be calculated either as a function of time or as an average over

TURN-ON:

h1	h2	k	x
7.69E-04	2.99E-02	2	-1.159

TURN-OFF:

m1	m2	n	y
1.76E-02	4.34E-02	1	-0.492

CONDUCTION:

Vt	a	b
0.51	0.46	0.649

Table 1. Power loss estimation parameter for IGBT in example

one period of current either using a spreadsheet or from closed-form solutions. Power losses so calculated can then be used to estimate temperatures of components inside the module, using specified thermal resistance numbers.

EXAMPLE

For a 1 HP (@ max. voltage) induction motor, supplied from an inverter with a DC bus of 400 V, the maximum RMS motor voltage would be about 226 V line to line with a modulation index of 0.8. Then the inverter output current per phase is about 3.2 A RMS (4.53 A peak) with a power factor of 0.6. This current can be expressed approximately as:

$$I = 4.53 \sin(\omega t) \quad (14)$$

The loss parameters for the IGBT under question are as given in the Table 1. Knowing the switching frequency, the energy losses can be averaged per switching cycle giving power loss per switch cycle. For purposes of calculation, the current can be approximated to be constant for one switching period. This is shown in the figure 5. Assuming that the current varies linearly within one switching cycle and the variation is small, the average current in the switching cycle can be assumed to be constant throughout the switching period. The value of the average current then varies sinusoidally between switching cycles as given in equation 14. The switching energies at turn-on and turn-off, and the conduction drop can be calculated for each switching cycle using equations 13 and 14. For each switching cycle, the average power loss including switching and conduction power loss, can be calculated giving a time-variant power loss as shown in figure 6. This figure shows power loss variation for half a modulation cycle i.e. for one IGBT. Knowing this, the average power loss can be easily calculated per IGBT and for a 3-phase inverter system.

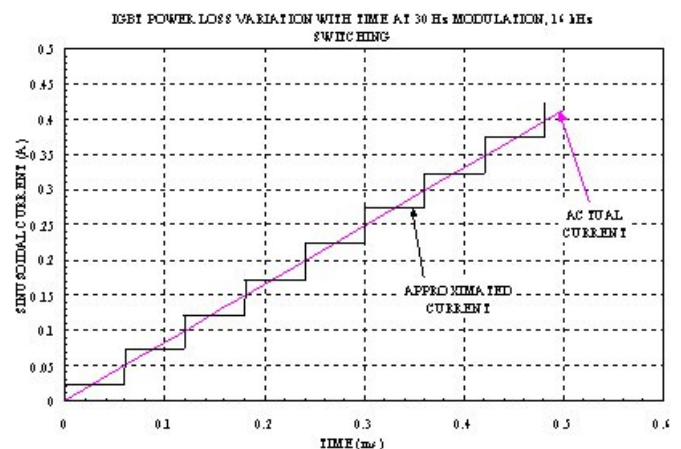


Figure 5: Plot showing approximation of sine current for loss calculation purpose

THERMAL RESISTANCE IN MODULE

Thermal issues in power modules can be different that those usually found in discrete parts. This is due to interaction between the heat flow paths of individual die within the power module. Figure 7 simplistically represents the thermal scenario for a power module containing multiple power dissipating IGBTs and diodes. All the die are mounted on a single substrate, which serves to electrically isolate the high voltage devices from the case of the module. The substrate, in most cases, unfortunately also presents a high thermal resistance to the flow of heat to the heat sink. As shown in the figure, heat spreads away from the power die at an angle that depends upon many factors including substrate material and quality of interface with the heat sink. Usually it is approximated to about 45 ° on all the sides of the die. It is easily seen from the figure that the heat dissipated through the region 'A' of the substrate increases as more die start to dissipate. Thus the effective thermal resistance of each power die as seen from the module case increases with number of dissipating die. The rate at which the effective thermal resistance increases with number of dissipating die depends on the heat-spread angle, the closeness of power die in the module and the actual power dissipated.

An example of effective thermal resistance variation with number of conducting die is shown in figure 8. These results were obtained from a finite element thermal simulation performed on a substrate bearing IGBT/diode die. The thermal resistance for an IGBT under such circumstances varies significantly from the case with one IGBT dissipating to that with all six IGBTs in 3-phase inverter configuration dissipating. It should be noted that even though the IGBTs do not actually dissipate DC power simultaneously, the thermal

time constants for the system are long enough for heating effects to be similar.

The power die in IRAMS modules are optimally located so that thermal interaction between them is minimal. Also, the thermal resistance R_{THJ-C} specified in the IRAMS datasheet is under actual running conditions with all the IGBTs and diodes dissipating power. A good estimate of the minimum value of R_{THJ-C} can be made using the physical dimensions and thermal properties of the module layers. An example of this using a spreadsheet model is shown in table 2.

In the table, assuming a heat spread angle of 45 ° on all sides of the die, the equivalent area of heat conduction can be calculate odule stack-up. Then knowing the material thermal resistivity, the thermal resistance to heat flow path can be calculated. Starting from the active silicon area with dimensions given by side 1 and side 2, and the thickness of material, thermal resistance for that layer is given by

$$R_{TH} = \frac{\rho \cdot t}{(side1 + \Delta x)(side2 + \Delta y)} \quad (15)$$

where t is the thickness of silicon, ρ is the thermal resistivity of silicon, Δx and Δy account for the 45 ° spreading of heat through the silicon die. Similarly, thermal resistances can be calculated for each layer in the stack-up as shown. The sum of all these thermal resistances gives the total thermal resistance of one IGBT to the module case.

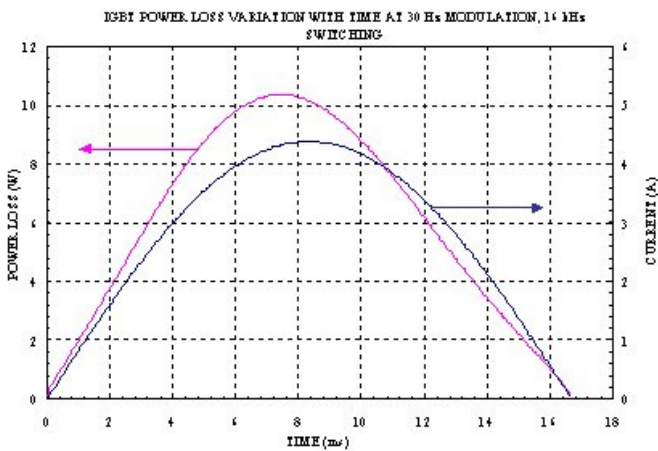


Figure 6: Variation of individual IGBT power loss with time

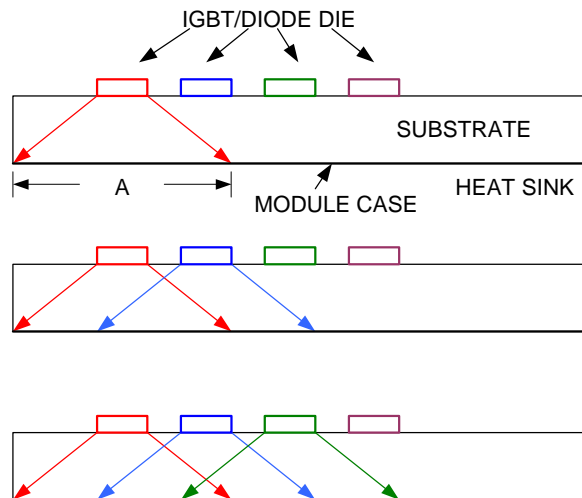


Figure 7: Heat propagation through back case for single and multiple dissipating die

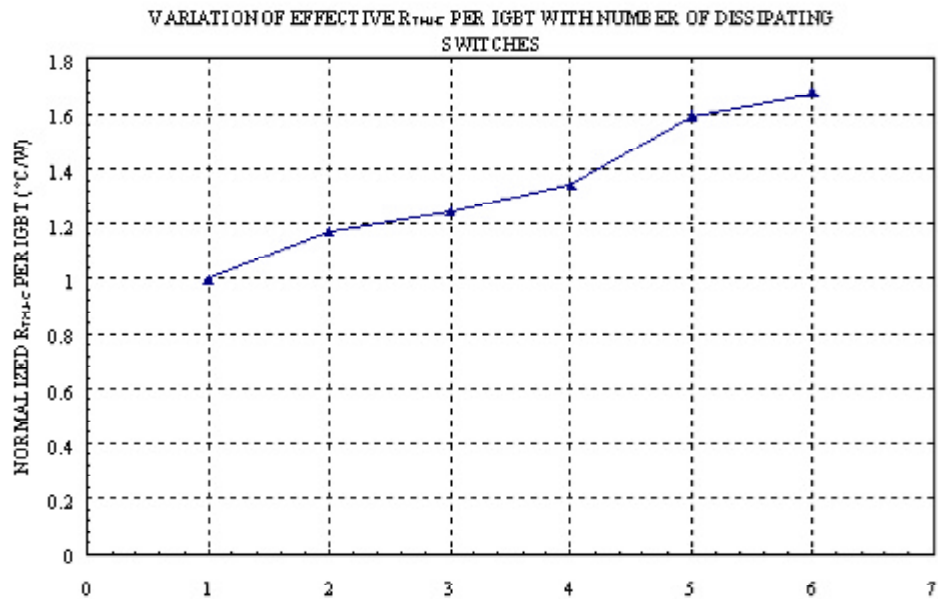


Figure 8: Variation of effective IGBT thermal resistance with number of dissipating die

Dimension	Side 1 inches	Side 2 inches	Side 1 m	Side 2 m	Area m ²	Thickness m	Rth $^{\circ}\text{K}/\text{W}$
Starting Active Area Silicon	0.080	0.080	2.03E-03	2.03E-03	4.13E-06	8.50E-05	0.18
	0.089	0.089	2.26E-03	2.26E-03	5.11E-06		
Solder	0.101	0.101	2.57E-03	2.57E-03	6.58E-06	1.00E-04	0.28
Copper	0.108	0.108	2.74E-03	2.74E-03	7.53E-06	7.00E-05	0.02
Dielectric	0.114	0.114	2.90E-03	2.90E-03	8.38E-06	5.00E-05	1.49
Aluminum	0.281	0.281	7.14E-03	7.14E-03	5.09E-05	1.50E-03	0.14
HTC Plastic	0.326	0.326	8.28E-03	8.28E-03	6.86E-05	4.00E-04	2.34
Zth Total							4.45

Table 2. Spreadsheet model to calculate IGBT thermal resistance in power module

Thermal Design (heat-sink selection)

The choice of heat-sink begins with the choice between free convection and forced air cooling. For the lower powered appliance drives, such as washing machines, the motor drive is located near the base of the enclosure and free convection is usually employed. Refrigerators and air conditioners use a condenser fan which can provide additional forced air cooling for the heat-sink. Heat-sinks designed for free convection airflow have taller, wider spaced fins than those for forced air operation and are about 50% larger for a given thermal resistance than a forced air heat-sink. The next consideration is the actual power to be dissipated and the allowable temperature rise above the ambient air temperature. This results in an overall thermal resistance value in degree per watt which usually specifies several possibilities of fin configuration and lengths of heat-sink extrusion. The designer then chooses the most suitable heat-sink to comply with the mechanical constraints of the application. In any system having a heat source and a final heat-sink, in this case the semiconductor die inside the module and the ambient air, there has to be a temperature difference ΔT which causes heat flow and a thermal resistance which determines the magnitude of the heat flow. An equivalent electrical circuit is shown below:

$R_{die\ attach} + R_{copper} + R_{insulation} + R_{substrate} + R_{molding\ compound}$ are lumped together to form $R_{th(j-c)}$ stated on the data sheet for each leg of the 3 phase inverter. $R_{case-sink}$ typically adds another $0.1^{\circ}C/W$ with a correct application of thermal compound such as Wakefield Engineering # 120 HS Compound. The peak junction temperature where allowable power dissipation derates to zero is $150^{\circ}C$ as stated on the data sheet. A prudent design would operate this module within a temperature range of T_j not exceeding $125^{\circ}C$ worst case.

Thermal Diagram

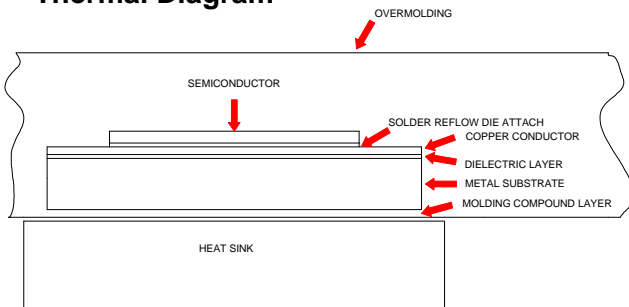


Figure 9: IRAMS module thermal diagram

Design Example:

Operation of a 750Watt A/C compressor from a 400VDC regulated bus (boost topology PFC) using the IRAMS10UP60B module driven at 3.3KHz. The worst case ambient temperature is $40^{\circ}C$ max. What heat-sink should I use to maintain $T_j\ max = 125^{\circ}C$?

The maximum obtainable voltage from a 400VDC bus assuming 80% modulation depth is 320V p-p. and the rms voltage equivalent is $0.707 \times 160 = 113VAC$ per phase. To generate 750W from 113VAC, the average current is 3.1A.

From the power loss calculation method described earlier, the following results are obtained for the above example:

Average switching power loss per IGBT $P_{sw} = 0.32\ W$
 Average conduction power loss per IGBT $P_{cond} = 1.49\ W$
 Average power loss per diode is $P_d = 0.53\ W$
 From the above numbers, total power loss including all 6 IGBTs and diodes is $P_{tot} = 14.1\ W$

IGBT thermal resistance from junction to case for the module IRAMS10UP60 is $4.7^{\circ}C/W$ as specified in the datasheet. It is assumed that heat is transferred to the heat sink uniformly from the module case. Thermal resistance from the module case to heat sink is approximately $0.1^{\circ}C/W$. Then the temperature rise of the IGBT junction above ambient is given by the following equation:

$$T_j - T_A = R_{THJ-C}(P_{SW} + P_{COND}) + P_{TOT}(R_{THC-S} + R_{THS-A}) \quad (16)$$

Substituting the above numbers in equation (16) with a desired T_j of $125^{\circ}C$ and an ambient of $40^{\circ}C$, the thermal resistance of the heat sink to ambient comes to $5.42^{\circ}C/W$. The heat sink shown in figure 11 is a standard part from Aavid/Thermalloy # 66365. With 3-inch length, it gives a thermal resistance of $5.38^{\circ}C/W$ from heat sink to ambient in free air convection. Thus the maximum junction temperature requirement is met.

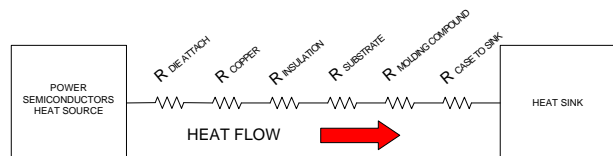

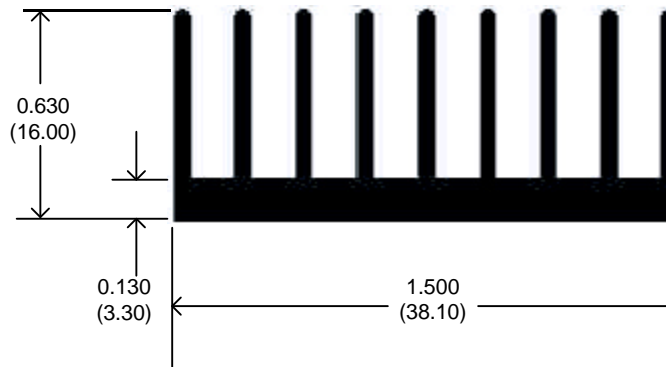


Figure 10: Electrical equivalent model

	Part Number	Thermal Resistance °C/W at 3in length	Width in	Height in	Surface Area in ² /in	Weight lb/ft	Part Class
	66365	5.38	1.50	0.63	13.00	0.50	B



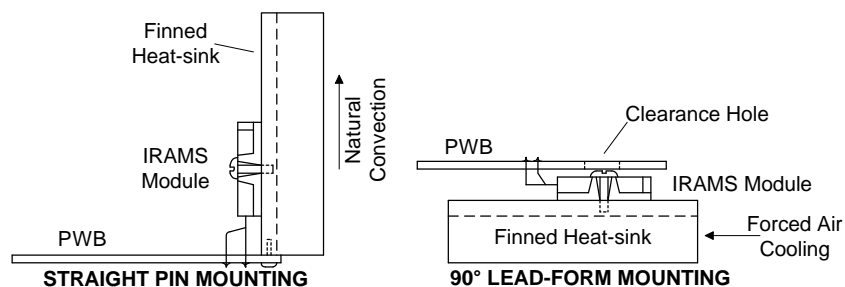
Packaging and Installation Guide.

The IRAMS modules are intended to be soldered into a printed circuit board, which in most cost sensitive products means a single sided PCB. Some inverter layouts, typically those used with natural convection cooling in washing machines, mount the heat-sink vertically at one edge of the circuit board using the straight pin version of the module. Forced air cooled applications such as split system air conditioners commonly mount the PCB parallel to the heat-sink using the 90° bent pin module configuration. The module mounting screws are then made accessible through clearance holes drilled in the PCB positioned above the module.

Mounting screws can be 6-32 NC or M3 torqued to a nominal 6 inch-pounds. The mounting surface of the module is electrically isolated by a thin layer of thermally conductive molding compound. The thickness of this layer is

carefully controlled during the molding process so that a uniformly low thermal resistance (3°C/Watt) can be maintained.

A heat-sink compound such as Wakefield Engineering #120 applied in a thin layer is strongly recommended for maximum heat flow into the heat-sink. However, for low power applications it may be omitted. Without heat-sink compound, the flatness and surface finish of the heat-sink greatly influences the thermal resistance of this interface. The mounting force also affects thermal resistance, so it is important to torque the mounting screws to 6in-LB or 0.7 Nm to ensure adequate contact. Spring clips can also be used to apply the required mounting force and provide a cost effective alternative to screw mounting when used in large volume production.



THE SYSTEM SCHEMATIC

A typical appliance or small industrial motor drive is shown in Fig. 13. The micro controller provides all of the logic level PWM signal inputs to the IRAMS module as well as processing current and temperature analog signals fed back from the module. The system schematic also demonstrates the simplicity of the drive and the small number of additional external components required. Note that no high-side floating power supplies are required because the bootstrap capacitors provide power for the three independent high side driver channels.

Motor current is monitored by external current sensing resistors in each phase leg of the IGBT inverter, but if ground fault detection is not required, a simplified current sensing can be provided by a single sense resistor. Under normal operating conditions, IGBT temperature is continuously monitored by the internal NTC thermistor feeding a temperature dependent voltage to the micro processor. This voltage also feeds the internal shut down function of the

driver which terminates all 6 drive signals when activated. In the event of an over current caused by a stalled motor or other fault condition, the active low signal from the micro controller turns off the external N-channel MOSFET and over rides the temperature signal causing instant shut down. After shutdown the 1.5Ω/6.8nF network provides a reset function to re-establish IGBT gate drive following a 9mS delay. The micro processor can be programmed to provide permanent termination of its outputs following a predetermined number of resets.

The sections so far described aspects of the system that directly affect the power module operation or selection, like bootstrap circuit, power losses within the module and thermal issues within and outside the module. The next sections briefly explain elements of the system that, no doubt, are important but do not determine or are not determined greatly by internal features of the module. These include the housekeeping power supply and DC bus capacitors.

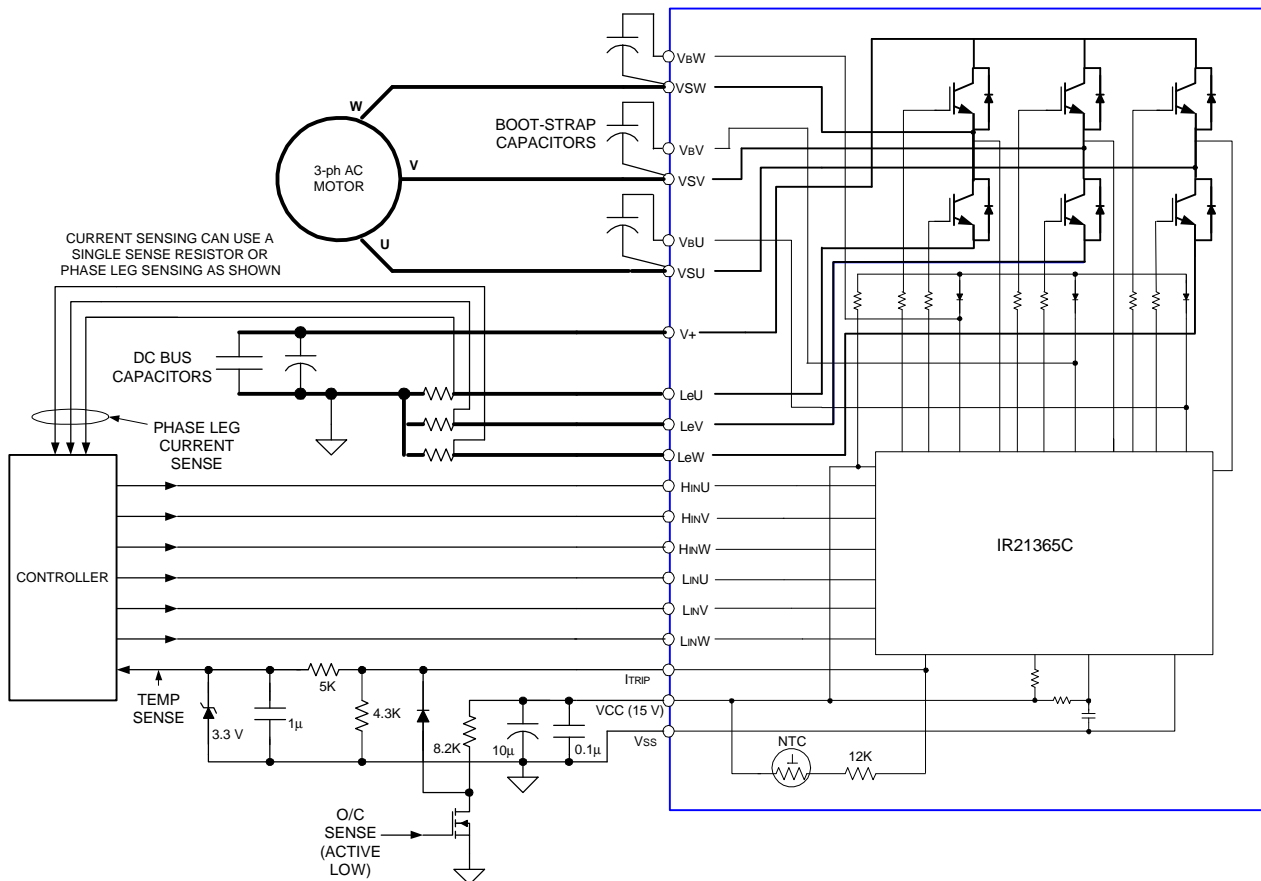


Figure 13: Typical system application

Bus Capacitor calculation

An electrolytic capacitor is used to smooth the rectified AC voltage from the bridge rectifier. Its capacitance is an inverse function of the allowed ripple voltage DV and can be derived from equation (17) below.

$$C_{\min} = \frac{2P_m}{(V_{\max}^2 - V_{\min}^2)f_{\text{rect}}} \quad (17)$$

Where P_m is the load power in watts and DV is $V_{\max} - V_{\min}$.

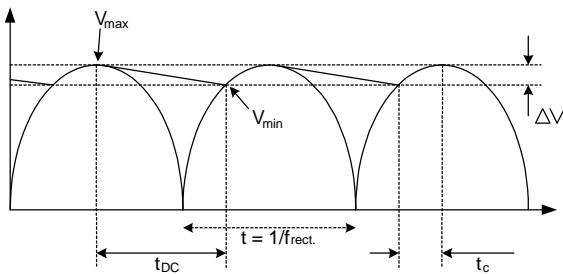


Figure 14: Rectified AC Waveform Showing Conduction period from Vmin to Vmax.

It should be noted that electrolytic capacitors age and lose some capacitance over time and that the tolerance of the initial capacitance value should also be considered at the time of selection.

When using a capacitive input filter, the capacitor value not only determines the ripple voltage but also the conduction angle of the rectifier. The input voltage is sinusoidal and the expression (18) shows the charging time:

$$t_c = \frac{\cos^{-1}\left(\frac{V_{\min}}{V_{\max}}\right)}{2\pi f_{in}} \quad (18)$$

where f_{in} is the line frequency.

The capacitor voltage discharge time t_{DC} can also be calculated from equation (19) below.

$$t_{DC} = \frac{1}{f_{\text{rect}}} - t_c \quad (19)$$

The average value of the charge current is given by:

$$I_{C_{\text{peak}}} = C \frac{\Delta V}{t_c} = C \frac{V_{\max} - V_{\min}}{t_c} \quad (20)$$

Equation (20) defines the average current drawn from the input rectifier and will be used in the selection of the rectifier diodes.

$$I_{C_{\text{rms}}} = \sqrt{I_{C_{\text{peak}}}^2 t_c f} \quad (21)$$

The rms current can also be calculated using equation (21) below.

$$I_{DC_{\text{rms}}} = \sqrt{I_{DC_{\text{peak}}}^2 t_{DC} f_{\text{rect}}} \quad (22)$$

The rms ripple current in the capacitor is given by equation (23) below.

$$I_{RMS} = \sqrt{I_{CRMS}^2 + I_{DC_{\text{RMS}}}^2} \quad (23)$$

The actual power loss in the capacitor is a function of its ESR at the ripple frequency of 100Hz or 120Hz depending on the mains frequency.

$$P_{\text{LOSS}} = I_{RMS}^2 \text{ESR}_{100\text{Hz}} \quad (24)$$

Controlling Capacitor Over Voltage

Capacitors can be destroyed if they are exposed to voltages in excess of their ratings due to line transients etc. An over voltage can also occur when capacitors are connected to an LC- filter. See Figure 15.

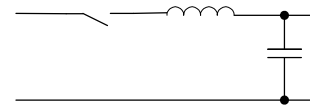


Figure 15: Capacitor ring-up in L-C Circuit.

The ringing waveform is shown in Figure (16) below.

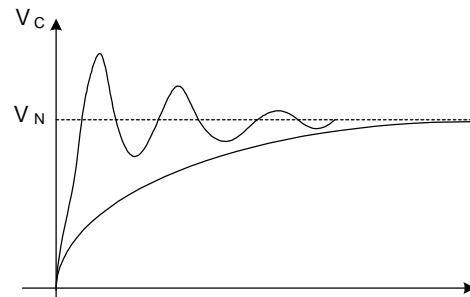


Figure 16: Voltage over shoot on the capacitor due to LC ring-up.

To avoid the voltage ringing when connecting the capacitors to the input network, it is advisable to use a soft start technique. Figure 17 shows two soft start networks. The soft start network 17(a) uses a self heating NTC thermistor or Surgistor for low power applications such as washing machines. For higher power applications up to 2.5KW, the circuit of (17)b can be used. A current inrush limiting resistor R is used and then shorted by a relay contact when the charging current decays.

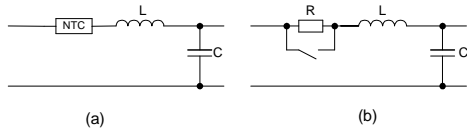


Figure 17: Soft start networks to avoid capacitor voltage overshoots

Auxiliary Power Supply

In the appliance motor drive the auxiliary power supply provides 3.3VDC or 5VDC power to the micro controller and supplies +15V bias to the IGBT gate drivers and other users such as relays and indicator LEDs. Individual systems may have variations but the most common solutions use +5V and +15V auxiliary power. In some cases, these voltages are required to be floating to prevent circulating currents in their return connections.

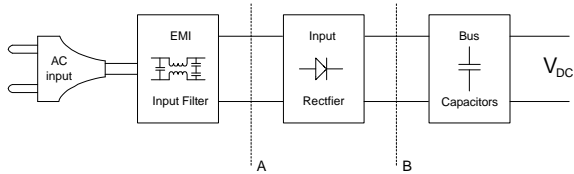


Figure 18: Power input path

Loads may be inserted at either point A or B depending upon whether an AC/DC or DC-DC converter is used to supply auxiliary power to the system as shown below in Figs. 19 and 20.

The AC-DC solution may be implemented by three different configurations. Fig. 19a shows the tradi-

tional AC solution where the transformer turns ratio defines the isolated DC bias voltage supplied by the bridge rectifier and capacitor. Of course, the output is unregulated and tracks the input line variations. Fig. 19b shows a non-isolated AC-DC step down approach suitable for low power bias applications. A dropping resistor provides the current source and the zener diode provides shunt regulation for the output voltage. Fig. 19c provides the most efficient solution, regulating the output voltage for line and load variations. Since this is a high frequency PWM solution, the transformer size can be greatly reduced compared with the mains frequency solution.

The DC-DC solution may be also implemented by three different configurations. Fig. 20a is a linear regulator providing 15V bias, but this circuit suffers from the same high dissipation problem as the circuit of Fig.19b . It would dissipate 120W with a 0.4A load. The PWM solution is the most efficient and reliable way to provide the bias voltage as shown in Figs. 20b and 20c. The buck configuration provides the non isolated approach, while the fly back configuration provides isolated outputs. The buck converter is the most efficient DC-DC converter and stresses the switching element to V_{in} but is non isolated. The flyback circuit stresses the primary switch to input voltage + reflected output voltage + leakage inductance voltage spikes which are attenuated in a dissipative snubber or spike clipper circuit. A typical flyback converter with 300VDC input requires a switch rating of about 800V.

The main DC bus filter capacitor attenuates the switching noise injected back to the input line by the PWM converter. This is a big advantage compared with the AC-DC solution of Fig.19c

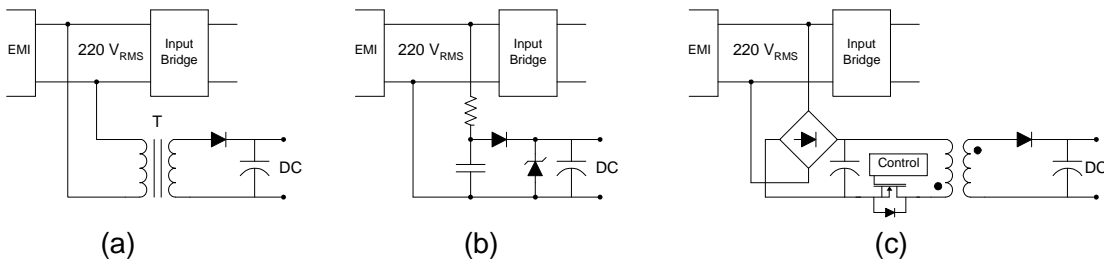


Figure 19: AC-DC insertion in the input path.

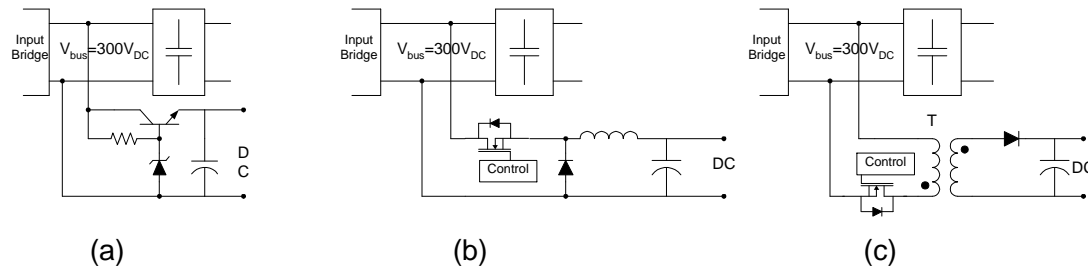


Figure 20: DC-DC insertion in the input path.

Power Analysis

To define the power requirements of the auxiliary power supply we need to evaluate the sources of power loss.

- Drive losses for the power switches.
- Power requirements for signal generation.
- Driver IC quiescent losses and level shift losses.
- Bootstrap diode loss.
- Other losses such as indicator LEDs and relays etc.

Since there are 6 IGBT switches, the drive losses P_s are:

$$P_s = 6 \times Q_g \times V_{ge} \times f \quad (25)$$

Where Q_g is the charge needed for one turn on turn off cycle of one IGBT, V_{ge} is the amplitude of the gate emitter voltage and f is the PWM frequency. In a worst-case scenario the value Q_g is 80nC in the module family, the maximum allowed gate voltage is 20V and the frequency in the appliance application is a maximum of 20kHz. Conductor power loss in bootstrap diodes is given by :

$$P_d = 3 \times Q_d \times V_d \times f \quad (26)$$

where Q_d is the charge delivered through the bootstrap diode to charge the bootstrap capacitor. V_d is the diode drop and f is the PWM frequency. These diodes are contained within the module so all the diode parameters are defined and fixed in the IRAMS data sheet. The Q_d value is 100nC, the maximum forward voltage is 1V and the frequency value is still 20kHz. Substituting in equation (26)

$$P_d \approx 6mW.$$

The total power dissipated at the IC drivers is:

$$P_t = P_s + P_d + P_{ic} = 200mW + 6mW + 100mW = 306mW \quad (27)$$

A reasonable design safety margin, would be to double the result in equation (27) plus some auxiliary power for signal conditioning. This gives a total power estimate of < 1W for the 15V auxiliary power supply.

An estimate of the power requirements for the control function using a micro controller and E²prom or a Pic microprocessor would be about 1W. To process the feedback signals some signal conditioning circuitry has to be added around the controller. A good estimation is 0,5W for the peripheral circuitry. The total 5V power is about 1.5W to the control section.

The IR Solution

Since the Plug N Drive module incorporates its own level shifting, 3 phase driver, the auxiliary power supply can be referenced to the negative bus and does not require isolated outputs.

Consumer applications are very much cost driven so the non isolated buck solution is very attractive.

Buck Converter Design

A Synchronous buck topology will be shown using the IR 2153 IC. This is a 600V, high speed, self-oscillating level shifting driver with both high and low side referenced output channels. The front-end features a programmable oscillator similar to the ubiquitous CMOS 555. The output drivers feature a high pulse current buffer stage and an internal dead time designed for minimum driver cross conduction when driving MOSFETS in a ½ bridge or synchronous buck configuration.

Using the estimates from equations (1) thru' (3) above, Table 1 gives a total power output for the auxiliary power supply of 4.8W.

	Power (W)
IC driver	0.3
Control Section	1.5
Linear Regulator 15V - 5V	3.0
Total	4.8

Table 3 Output Requirements of Auxiliary Power Supply

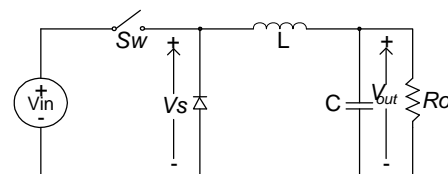


Figure 21: Buck converter circuit

The output voltage of an ideal buck converter is a function solely of input DC voltage and duty cycle D , so long as the inductor L is in continuous conduction.

$$V_{out} = V_{in} \times D$$

In a practical circuit the components have losses so the relationship becomes:

$$V_{out} = \langle v_s \rangle = \frac{1}{T_s} \int_0^{T_s} v_s(t) dt = \frac{1}{T_s} (DT_s V_{in}) = DV_{in} \quad (28)$$

In operation, the amplitude of the switching voltage V_s is equal to the input DC voltage minus the switch saturation voltage drop V_{sw} plus the diode forward conduction voltage V_f in times respectively switch on and off. A specification for the auxiliary power supply is shown below in Table 4.

Power Supply Specification

Parameters	Min.	Max.
Input Voltage	40V	350V
Output Voltage	14.5V	15.5V
Load value	37.5W	56.5W
Output Power	4W	6W

Table 4. Power Supply specification

For practical purposes, the maximum duty cycle obtainable from the IR2153 is about 45%. Using the values shown in Table 4, the minimum input voltage is:

$$V_{in_{min}} = \frac{V_{out}}{D_{max}} = \frac{15V}{0.45} = 33.45V \quad (29)$$

At the other end of the scale, the DC bus voltage from a boost topology PFC preregulator is up to 400V. The duty cycle corresponding to this condition is determined from equation (30). Thus we can confidently predict that the auxiliary power supply can operate safely from a DC input of 40V to 400V.

$$D_{min} = \frac{V_{out}}{V_{in_{max}}} = \frac{15V}{400V} = 3.75\% \quad (30)$$

The IR2153 self oscillating driver IC uses the values of R_T and C_T to determine its oscillation frequency. Its supply volt-

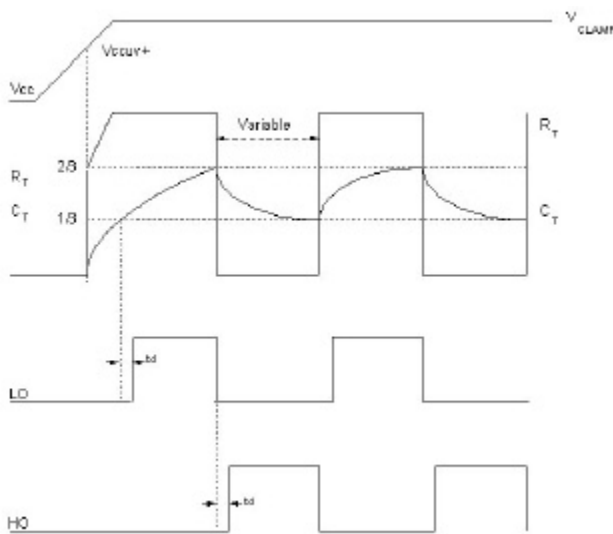


Figure 22: C_T waveform and Output Timing Diagram of IR2153

age V_{cc} is internally regulated to 15.5V and switching takes place at $1/3$ and $2/3V_{cc}$ just as in the generic 555 timer. The oscillator frequency is shown below :

$$f = \frac{1}{1.4(R_T + 150\Omega)C_T} \quad (31)$$

The Regulator Control Loop

Referring to Fig. 23 below, we see that the complete regulator schematic includes a TL 431 programmable shunt regulator IC. This regulator produces a high gain control loop and controls the duty cycle as a constant off time regulator. The high side switch duty cycle is large when the input voltage is low and small at high input voltage. Thus it can be seen that the constant off time control results in low frequency operation at 33.45V input and high frequency operation at 400V input. It is also noted that the TL 431 bypasses some charging current from C_2 and thus increases its charge time to maintain voltage regulation of the +15V output. If we choose to operate at 50KHz and, the values from equation (31) are:

Under these conditions we see that:

$$R_T = 5.1k\Omega$$

$$C_T = 2.7nF$$

$$\begin{aligned} D_{max} &= \frac{T_{on_{max}}}{T_{on_{max}} + T_{off}} & T_{off} &= 11ns \\ D_{min} &= \frac{T_{on_{min}}}{T_{on_{min}} + T_{off}} \text{ and } T_{on_{min}} &= 507ns \\ f_{sw_{min}} &= \frac{1}{T_{on_{max}} + T_{off}} & f_{sw_{max}} &= 99kHz \end{aligned} \quad (32)$$

Inductor Calculation

In continuous conduction, the minimum inductance value is given by equation (33) below.

$$L_{min} \geq \frac{R_{out_{max}}(1 - D_{min})}{2 f_{sw_{min}}} = \frac{56.5\Omega * (1 - 0.05)}{2 * 50kHz} = 537nH \quad (33)$$

In order to select the correct inductor the inductor peak current has to be calculated by the expression (34)

$$I_{pk} = \frac{V_{out}}{R_{out_{min}}} + \frac{T_{off} V_{out}}{2L} = \frac{15V}{37.5\Omega} + \frac{11ns * 15V}{2 * 600nH} = 0.54A \quad (34)$$

General Low Side Current Sensing

Introduction

The low side emitters, in the IRMAS10UP60A, are not tied together, which allows either the micro controller or the DSP to monitor the currents by external current sensing resistors in each phase. The purpose of these notes is to show a peculiar solution for feeding the current feedback to the A/D converter in the control scheme.

Problem analysis

When the shunt resistors are connected between the IGBT emitter and negative bus (Vbus-), the phase current is sensed in each leg. Figure 25 shows a typical schematic

The voltage signals are easier to be manipulated than current signals, so the shunt resistor works like a current to voltage transducer.

In a typical motor drive application, the voltage sensed by the shunt resistor can be either positive or negative when referred to the Vbus-. The A/D converter must have positive input signals only. This is a big limitation and doesn't allow the designer to use the shunt voltage information directly.

Solution

The signal supplied by the shunt resistor has to be compatible with the A/D input dynamic. It needs to be offset by a suitable value, thus the obtained signal is positive in all the current range. For instance the transfer function might be like the one shown in Figure 26.

Such transfer function can be implemented by the schematic shown in Figure 24. It is a peculiar differential amplifier with two inputs signals. The first one is the differential mode value and the second one is the offset value.

Some assumptions were done to have a simple expression of Vo/Vin. Figure 24 reports the relationships among the resistors in order to have:

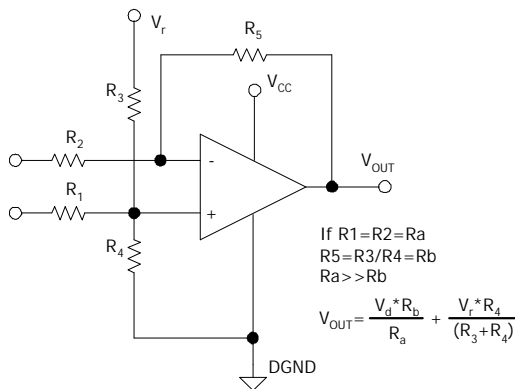
$$V_{out} = V_d \frac{R_b}{R_a} + V_r \frac{R_3}{(R_3 + R_4)} \quad (35)$$

Where V_d is the input signal or the shunt resistor drop, $R_b=R_5$ and $R_a=R_2$ select the voltage gain, V_r and the ratio $R_3/(R_3+R_4)$ set the input offset needed.

The final circuit performance is related to the op-amp characteristics. It has to be Rail-to-Rail input/output in order to use the entire output dynamic. It needs a GBW > 1MHz, good slew rate > 0.5V/μV and low input offset voltage. It might be too expensive, but for instance the TLV2460 fits the request of the application.

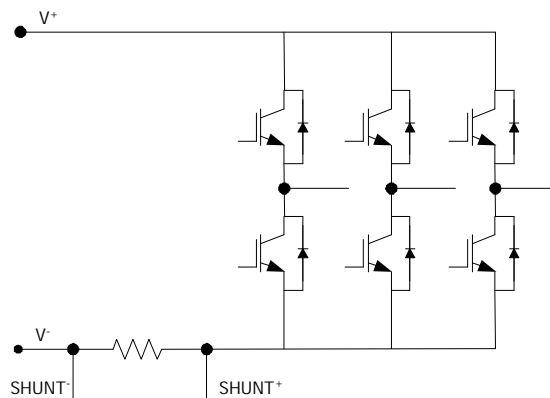
Two examples, useful for the IRAMS10UP60A application, are reported in this paper.

Figure 25 shows the typical three-shunt current feedbacks using the IRAMS10UP60 power module. The shunt voltage amplitude is related to the shunt value itself and the maximum current through it. The IRAMS10UP60A datasheet reports the max peak current allowed is 15A. As advised in the application note AN1044, the designer has to provide an external circuit that feeds the T/trip pin to shut down the system as soon as the current goes close to the max value. The pro-



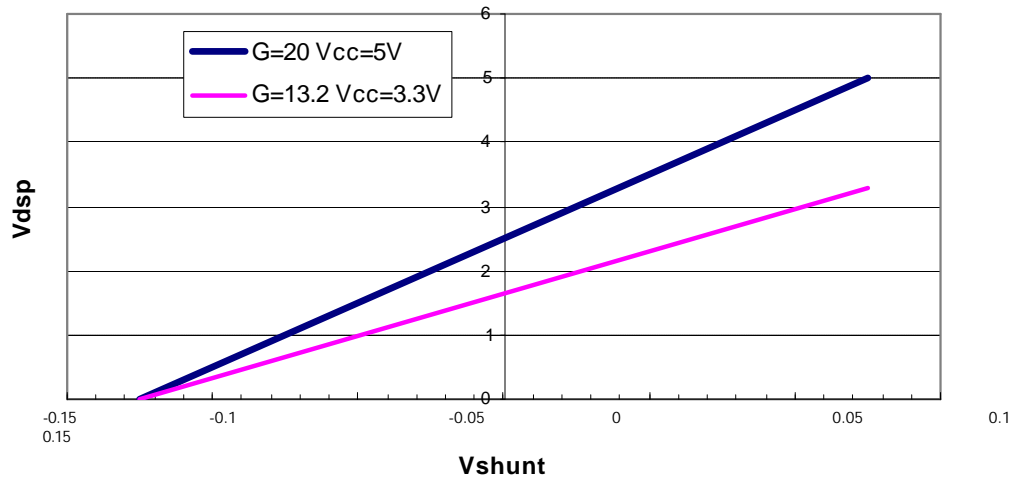
Current feedback Signal condition general circuit (Figure 24)

Typical example circuits



Typical low side current sensing circuit (Figure 25)

Vout vs. Vshunt in Current Feedback signal condition circuit



Signal condition transfer function (Figure 26)

tection loop must shutdown the system faster than 10 μs otherwise the IGBTs will not survive the fault.

Using a rail-to-rail op-amp the circuit can read current up to 12.5A using 10mΩ as shunt resistors. Figure 27 shows the final amplifier configuration when the logic circuitry at 5V. The voltage amplifier gain is 20. From the expression (35) the input voltage is:

$$V_{d\max} = \left(V_{outM} - V_r \frac{R_3}{R_3 + R_4} \right) \frac{R_a}{R_b} = \left(5V - 5V \frac{100k\Omega}{(100k\Omega + 100k\Omega)} \right) \frac{2.49k\Omega}{49.9k\Omega} = 0.125V \quad (36)$$

$$V_{d\min} = \left(V_{outm} - V_r \frac{R_3}{R_3 + R_4} \right) \frac{R_a}{R_b} = \left(0V - 5V \frac{100k\Omega}{(100k\Omega + 100k\Omega)} \right) \frac{2.49k\Omega}{49.9k\Omega} = -0.125V \quad (37)$$

The values in (36) and (37) define the input dynamic of the differential amplifier. Assuming that during the start up phase the system runs at 12.5A, the R_{SHUNT} is:

$$R_{SHUNT} = \frac{V_d}{I_{LEG}} = \frac{0.125V}{12.5A} = 10m\Omega \quad (38)$$

The expression (38) defines the R_{SHUNT} value in order to have a range of +/-12.5A in the application. The circuit suggested in Figure 27 has good bandwidth up to 50kHz. It is wide enough for current sensing. If the user wants to change it, he has to play with C2 and C3. Keep in mind that the relationship $Z_3 = Z_4$, in order to change C2 and C3, has to be maintained

The reader can do the same consideration on the circuit shown in figure 28 to evaluate the characteristics. Basically the circuit has the same performance of the circuit showed above using 3.3V voltage.

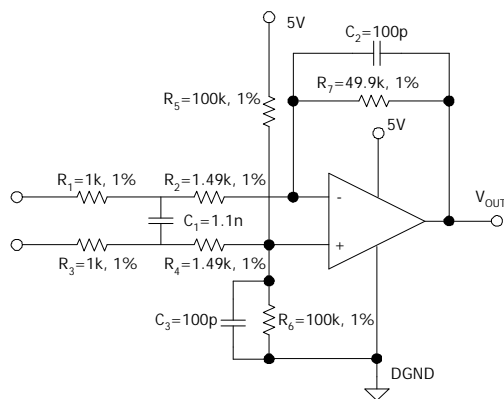


Figure 27: Current Feedback Signal condition circuit: Vcc=5V Gain=20

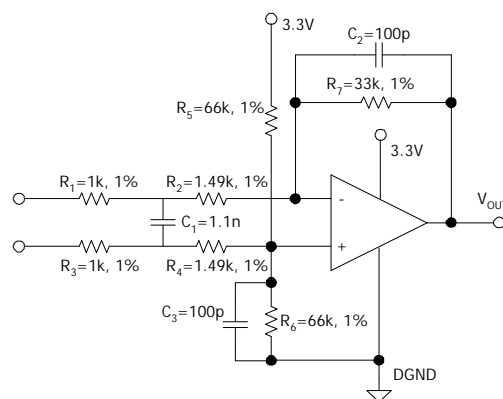


Figure 28: Current Feedback Signal condition circuit: Vcc=3.3V Gain=13.2

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