

# ***DirectFETä - A Proprietary New Source Mounted Power Package for Board Mounted Power***

*by Andrew Sawle, Martin Standing, Tim Sammon & Arthur Woodworth, International Rectifier, Oxted, Surrey, England*

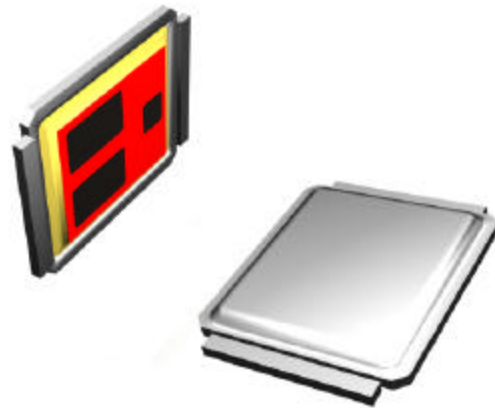
## **Abstract**

This paper will present a new power semiconductor product from International Rectifier called DirectFET™ for board mounted power applications. The DirectFET product breaks new ground in performance for die free package resistance and thermal resistance for an SO-8 comparable footprint. This paper details a new interconnect methodology which enables the DirectFET™ to achieve benchmark power density and efficiency in board mounted power applications.

## **Introduction**

In today's information technology driven age, increasingly complex software applications are demanding ever greater levels of processing power. This has led to continuing advances in processor technology resulting in more power hungry processors running at higher and higher clock speeds. In order to make these advances, silicon geometries are being ever reduced resulting in the supply voltage being forced lower. Consequently in order to maintain or increase processor power, the supply current is increasing which results in higher power densities on the board. These advances are challenging for the designers of the dedicated power supplies that are required to service these processors since these low voltages and high currents need to be tightly regulated. In addition, fast transient response is also required by the processor from the supply. In order for power supply development to maintain pace with that of the processors, designers are demanding power semiconductors with lower on-state, switching and thermal losses in order to maintain the same or reduced solution sizes and stable board temperatures. In addition, at the increased frequencies required for fast transient response times, board layout also becomes an important consideration since board parasitics can also add to system losses. Therefore designers are looking for power semiconductor solutions that allow them uncomplicated layouts located close to the processor itself.

Power silicon development in the low voltage devices required for board mounted power has until recently outstripped advances in power packaging. This has meant that designers have not been able to realise much of the gains made in silicon efficiency. However, recently the focus has been on the potential gains to be made in packaging efficiency and consequently the market has seen a number of innovative new products closely integrating the silicon with the package targeted primarily at board mounted power applications. In this paper, International Rectifier introduces a new, proprietary, surface mount product called DirectFET™, as shown in Figure 1.0.



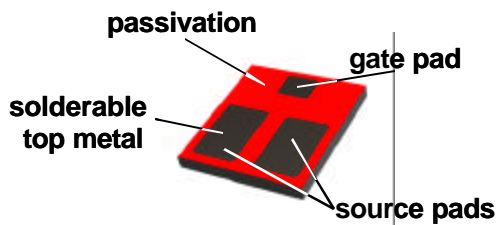
**Figure 1.0- DirectFETä**

The DirectFET has been developed to address the key demands made by board mounted power designers. These being lower conduction losses, improved switching and thermal performance and ease of paralleling for lower inductance board layouts. This paper will examine each of these areas in turn showing how through the use of a proprietary new interconnect technology, improvements over current power semiconductor solutions have been made.

## **New Interconnect Methodology**

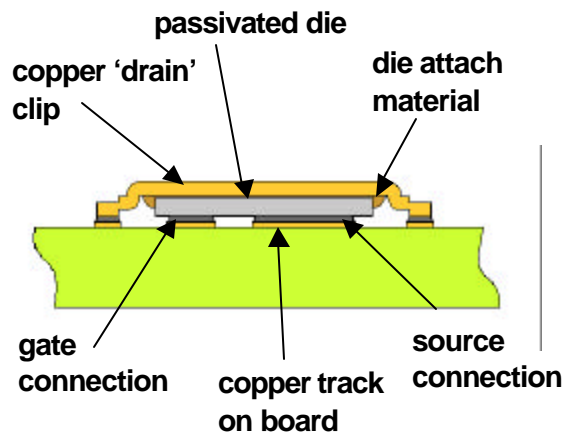
For a number of years there has been a move towards employing solder balls as an interconnect medium, first on ball grid array

packages and more recently on flipchips. This technology has allowed multiple connections to be made between the surface of a silicon die and a circuit board. Whilst this has facilitated reductions in product footprint size, reduced package related conduction losses and made gains in thermal performance there are still further improvements that can be made in all these areas. A ball grid array approach, even with multiple balls per connection has a limited contact area with a printed circuit board and hence the thermal performance junction to board and conduction efficiency cannot be maximised. International Rectifier has looked to offer an alternate interconnection methodology that addresses this issue and has developed a large area contact technique and employed it on the DirectFET product. By developing and using a proprietary passivation system and using it in conjunction with a MOSFET die that employs a top metal configuration that is solderable, large area solderable contacts have been created. One such example of this is shown in Figure 2.0.



**Figure 2.0– Solderable Contacts on DirectFET die**

The passivation plays two important roles. Firstly it separates and defines the source and the gate pads on the MOSFET die. The source and an enlarged gate connection can then be soldered directly to a printed circuit board. The passivation acts as a solder mask and prevents shorting between these two connections. A copper 'can' is then used to bring the remaining drain connection from the back of the silicon die down onto the printed circuit board. This concept is shown in cross-section in Figure 3.0.



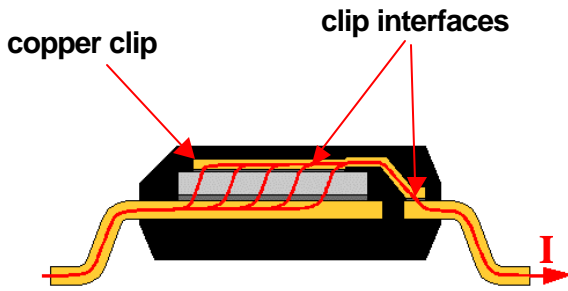
**Figure 3.0– Cross-section of DirectFET Soldered to PCB**

Secondly, the passivation protects the termination and gate structures of the die from moisture and forms of contamination and hence facilitates a product resistant to the environment.

By using this configuration with the junction of the die in close proximity with the circuit board a number of performance benefits can be realised. These advances will now be documented.

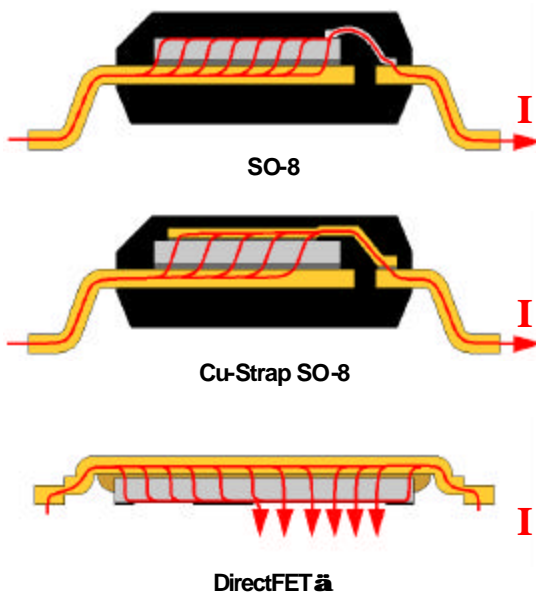
#### Conduction Performance

Traditionally, wirebond technology has been used to make electrical interconnections between the silicon die and the leadframe in power semiconductor packages. In order to reduce the package related conduction losses efforts have been made to employ many paralleled gold or aluminium wirebonds but there is a limit to the performance attributed too this technology. More recently products have been developed that eliminate the wirebonds through the use of a copper strap or clip that is soldered directly to the surface of the die and to the leadframe. Relative to wirebonds, the copper strap has a large cross sectional area which reduces the electrical resistance. Additional gains are made through reductions in the spreading resistance seen in the top metal of the die by having a high conductivity parallel path (the copper strap) soldered in place. However, the factors that limit the further reduction in on-state losses are shown in figure 4.0 below.



**Figure 4.0– Current Conduction Path for a Typical Clip-bonded SO-8 Package**

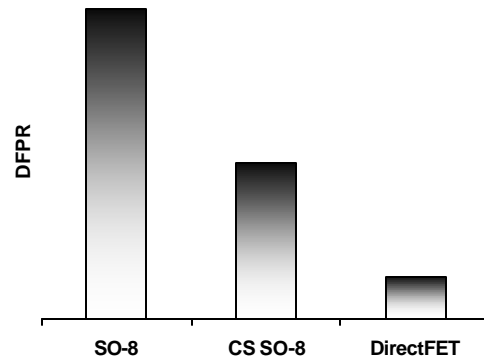
Even though the copper clip improves the conduction performance, the leadframe material and the materials used to attach the clip to the frame/die have inherent resistances equal in many cases to the  $R_{ds(on)}$  of the silicon that it services. In order to make further inroads into conduction losses it is necessary to reduce both the number of interfaces and the length of the leadframe conduction path. Both these concepts were employed during the development of DirectFET. Figure 5.0 shows a comparison of conduction paths between a wirebonded SO-8, a copper strap SO-8 and DirectFET.



**Figure 5.0– Comparison of Current Conduction Paths for SO-8, Cu-strap SO-8 & DirectFET**

The result of this rationalisation of the conduction path is shown graphically in Figure 6.0. This shows the relative die free package resistance

(DFPR) for the SO-8, copper strap SO-8 and a similar sized DirectFET.



**Figure 6.0– Graph Showing Relative DFPRs for SO-8, Cu-Strap SO-8 & DirectFET**

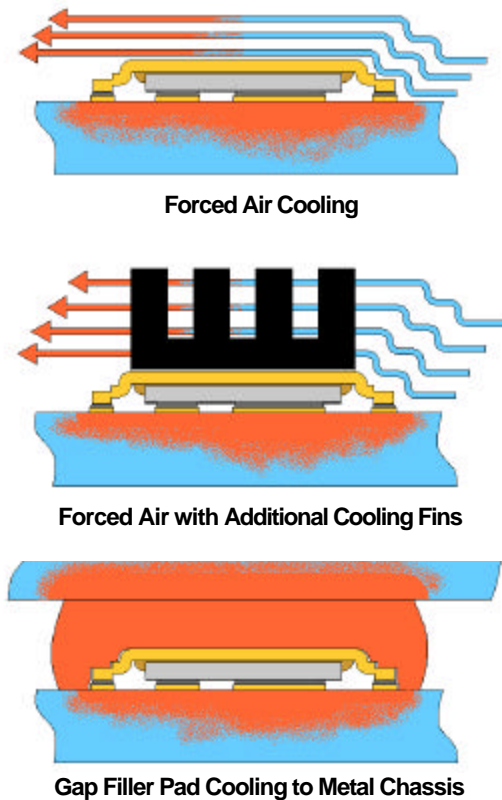
Numerically, the improvements in DFPR are approximately 86% over a conventionally wirebonded SO-8 and approximately 73% over a copper strap SO-8. This means that for an equal die size, DirectFET exhibits benchmark conduction performance for any commercially available SO-8 outline. This benchmark performance is replicated in any like for like comparisons in terms of die size for packages up to a D<sup>2</sup>Pak.

### Thermal Performance

Another area of performance improvement realised through the new interconnection technology is a large reduction in thermal resistance. This improvement can be seen by looking at two of the features of the DirectFET. Firstly, the  $R_{th(junction-pcb)}$  for this product is significantly lower than for a typical leaded small outline package. This is because the only materials in the thermal resistance path between the junction and the board are the top metal on the die and the solder used to mount the part onto the board. An example of the level of improvement achieved is that  $R_{th(junction-pcb)}$  for an SO-8 is approx 20°C/W but for the same footprint area DirectFET achieves <1°C/W.

A second important feature of the DirectFET is that the metal (and lack of plastic mould compound) can provide a low thermal resistance path between the junction of the die and the top of the package. This facilitates an ability to use top side cooling, either through forced air with or without additional fins or by

using a thermally conductive gap-filling medium to conduct to a suitable heatsink, chassis, etc. These concepts are shown in Figure 7.0.



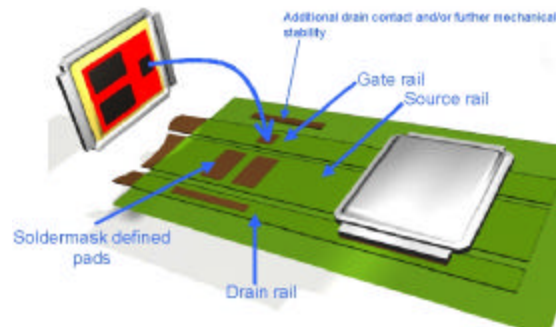
**Figure 7.0– Topside Cooling Examples for DirectFET**

As power densities on boards increase, the thermal considerations become ever more important. The ability to top-side cool means that heat dissipated can be pulled away from the circuit board, increasing the currents that can be safely carried by a single device.

### Switching Performance

As the operating frequencies of board mounted power applications increase and the response times demanded by the processor or its power supply decrease, the ability of a system to switch efficiently is important. This is governed by the efficiency of the silicon used, the inductance of the methodology used to make the necessary electrical connections between the die and the circuit board and the track layout on the circuit board itself. The DirectFET has been designed to tackle the induction issue in two ways. Firstly, by eliminating wirebonds and complex leadframe

geometries inductance is lowered. Secondly, one element of the design brief for the DirectFET was to develop a product that simplified board layout for paralleling devices and hence reduce board level inductance. The pad design has been laid out such that straight, parallel tracks can be used on a circuit board to parallel devices. By using an uncomplicated track layout it is possible to reduce the board contribution to unwanted system inductance. Figure 8.0 shows the pad layout that allows simplified paralleling of devices.



**Figure 8.0– Paralleling DirectFETs**

The improvements made in both the effective package inductance and the related board level inductance mean that board mounted power designers can increase the frequencies at which they switch their systems, improving efficiency and reducing the transient response times that the latest generations of processors require.

In addition, pad and gap dimensions have been designed to allow surface mounting on relatively large pitch assembly lines (0.01inch screen solder print) such as may be employed when assembling IMS or DBC substrates.

### Improvements in Die:Footprint Ratio

In addition to the conduction and switching efficiency improvements made through the development of the DirectFET product, the design rules used have meant that it has been possible to increase the die to footprint ratio. In simple terms this means that a greater percentage of the total product area is taken up by the silicon die. This is good news for the designer since really the silicon die is the 'useful' part of any power semiconductor device and the package part only facilitates connection to the silicon from the board. The less additional area (over that of the silicon) that the packaging of a product occupies then less expensive board real estate is wasted. The gains made in this area

mean that for the same package outline the DirectFET can house a more than 30% larger silicon area than the industry standard SO-8. This means that not only are there  $R_{ds(on)}$  gains to be made through the reduction in die free package resistance but the improved die:footprint means that for the same overall product area, the on-state losses can be radically cut by increasing the silicon area.

However, whilst the gains to be made in an SO-8 outline area are over 30%, the gains to be made over larger footprint products are even greater. Since the design rules governing the distances between the edge of the die and the edge of the metal 'can' do not change with die size then the larger the die the greater the die to footprint ratio will become.

The effect of these gains mean that designers will need to parallel fewer power mosfets in order to achieve the effective  $R_{ds(on)}$  figures that they require for their systems. This will aid reductions in system costs through facilitating reduced component counts which in turn will reduce the land area occupied by the power components thus saving board space This will also have a impact on assembly costs since fewer products will need to be placed onto the board.

Additionally, the DirectFET is able to make further space savings. Due to the nature of the unmoulded construction of the product, the profile is considerably less than that of similar small outline packages. The DirectFET has a height profile of 0.7mm, whilst an SO-8 is 1.75mm in height.

## **Conclusion**

This paper has presented a new power semiconductor product developed by International Rectifier called DirectFET. Through the use of a new proprietary passivation and interconnection methodology, radical gains have been made in both conduction and thermal efficiencies. In addition, it can be seen that the switching performance of a board mounted system can be improved by employing DirectFET since it allows easy paralleling of the MOSFETs on straight parallel tracks.

This new product, whilst targeted primarily at board mounted power and the SO-8 type outline is scaleable both up and down in size, allows board designers to make savings through reduced component counts and board real estate savings.