Increased Efficiency and Improved Reliability in “ORing” functions using Trench Schottky Technology

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Abstract – *Presented in this paper are the characteristics of the first Trench MOS Schottky Diode released to manufacturing by International Rectifier. The optimized Silicon structure enables 15% V_F reduction and a factor 4 of leakage suppression compared to a benchmark conventional planar device of the same voltage class. After reviewing the key features of Silicon design, the results of an in-circuit test are presented, indicating the advantage of using trench Schottky as OR-ing diodes in term of reduced power dissipation, reduced component count and improved ruggedness.*

I. INTRODUCTION

In Redundant (n +1) power supply configurations, “Hot-Swap” and “ORing” functions can be provided in three ways:

1) ‘Mechanical’ solution (screw-in, two-stage connector, capacitor and resistor).
2) Traditional Diode solution.
3) ‘Active’ solution (IC control with MOSFETs).

The paper investigates the advantages of Trench Schottky used as protection devices in “ORing” functions.

System reliability is dependent on correct component choice, component reliability & system implementation.

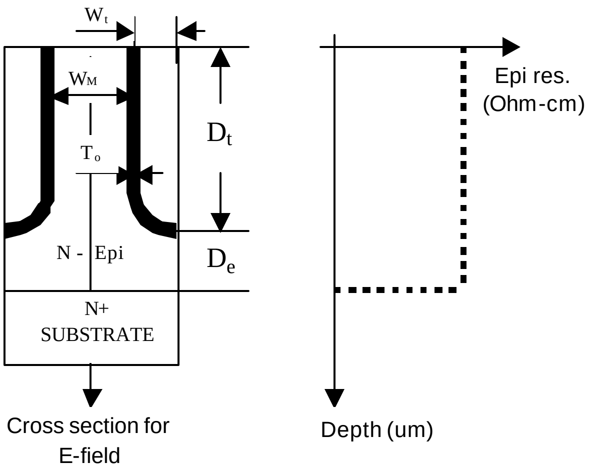
The silicon structure enables an improved forward voltage drop (V_F) and reverse leakage characteristic (I_R). This allows the device to operate with reduced Forward losses and increased Max Junction Temperature ratings than a planar device, thus reducing the heat dissipation and increasing the safety margin during operation.

II. DEVICE SIMULATIONS AND STRUCTURE OPTIMIZATION

The main requirement for a Schottky Rectifier used as OR-ing diode is the low forward Voltage Drop. At the same time a Max Junction Temperature rating $T_{j,max} \geq 125C$ is preferred, in order to avoid the thermal run-away in case of power supply failure in redundant systems.

Trench MOS Barrier Schottky (TMBS) is an attractive candidate for reducing power loss in the rectifier. The basic concept, first presented by Prof. Baliga [1], has gone through several experimental confirmations in low voltage [2], and high voltage devices [3]. Several Patent Applications have been recently issued. In order to improve reliability and protect the Gate Oxide from charge injection during deep depletion induced-avalanche, a clamping Diode in parallel with the Schottky has been proposed [4]. Improved terminations have been disclosed [5,6] and recently a more efficient device concept was proposed [7]. However, none of the above proposals has yet resulted in a manufacturable TMBS device.

In order to optimize Epi specs and trench depth, 2-D Device simulations were conducted using ISE



a) b)

Fig 1. Basic cell used for epi optimization simulations a), and simulated epi profile b).

Trench (Wt) and mesa width (Wm) were kept constant and equal to the minimum features allowed by the Photolithography Process.

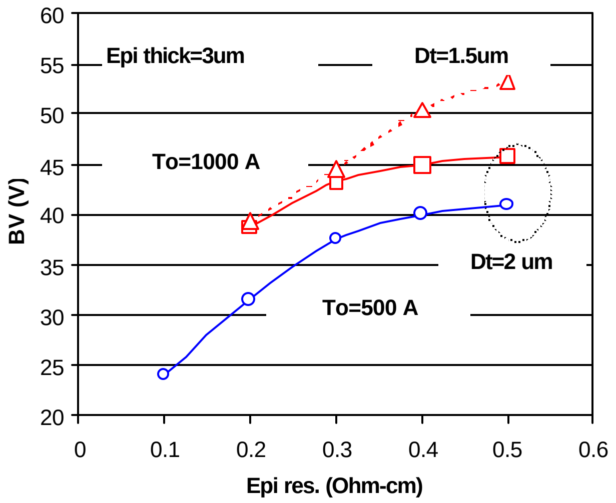


Fig 2. BV as a function of Epi res. for different To and Dt parameters.

A range of Epi resistivity between 0.2 and 0.5 Ohm-cm was considered in the simulation. Lower resistances (as in Ref 5) would lead to extremely high leakage due to the low Schottky barrier metal used in this case.

Fig. 2 shows that BV increases for oxide thickness (To) greter than 500A and increases for shallower trench and Epi res. ≥ 0.3 Ohm-cm. Epi thickness is fixed to 3um. These results indicate that the structure is punch-through for Epi res. ≥ 0.3 Ohm-cm, as confirmed by Fig. 3, where the electric field profile in the center of the mesa is plotted along a vertical direction.

The location of the maximum electric field is shifted from the surface, as expected in a conventional Schottky, to the trench bottom as described in Refs 1 & 3. The surface Efield, responsible for Image Force Barrier Lowering, decreases as Epi res. increases, indicating that higher resistivity would ensure complete suppression of Reverse leakage.

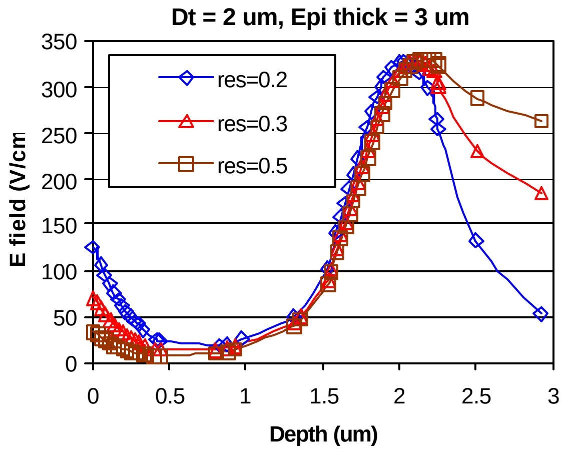


Fig 3. Electric field profile along a vertical direction in the center of mesa. Wm=0.5um, To=500A.

The structure is highly punch-through (Efield >0 at the epi / sub interface) for Epi res > 0.2 Ohm-cm. For this range of resistivity more than 50% of the voltage is dropped in the epi-region between the bottom of the trench and the substrate interface. Ergo, this introduces the possibility to optimize the structure by reducing epi thickness and trench depth while still keep the same breakdown voltage. The above consideration is valid for thicker oxide to > 500A, provided the Epi-resistivity is increased accordingly.

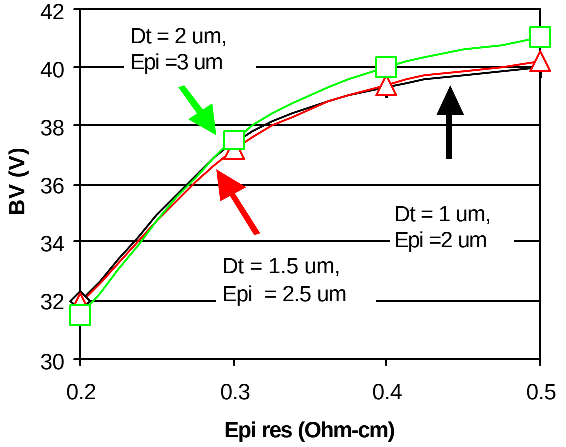


Fig 4. BV as a function of Epi resistivity, with De=1um. Wm=0.5um, To=500A.

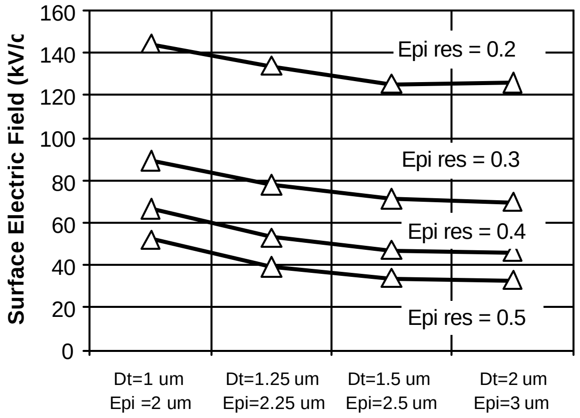


Fig 5. Surface Electric Field vs Trench Depth. Wm=0.5 um, To=500A, De=1 um. Epi resistivity values are expressed in Ohm-cm

The optimization results are shown in Fig 4. For a fixed resistivity, the same BV can be obtained by a shallower trench, as long as the parameter De, delta between epi thickness and trench depth, remains the same (= 1um in Fig 4).

In order to reduce the Vf and maintain a relatively high BV, a thin epi layer and shallow trench are preferred. The only drawback of this approach is the increase of Surface Field, responsible for reverse leakage (shown in Fig 5).

Here we summarize the results and indications of device simulations:

1) In order to reduce the Forward Drop and keep a low leakage, a combination of a low Schottky barrier metal, narrow (~ 0.5um) MESA width, thin Gate Oxide (~ 500A) and Epi-resistivity > 0.2 Ohm-cm is preferred.

2) In the above conditions, the structure is punch-through, and the Breakdown voltage is driven by the parameter De, the delta between the trench bottom and the epi / substrate interface.

3) In order to reduce the Vf, maintain the target BV, and not incur in surface field-induced leakage increase, a trench depth 1.5um < Dt < 2.0um is preferred.

III. EXPERIMENTAL RESULTS

A 15V rated TMBS was fabricated, by using a high density trench design. Stripe geometry was chosen in order to reduce the presence of sharp corners in the gate oxide which create electric field crowding and reduced ruggedness. A low barrier Schottky metal was used.

A cross section of the fabricated cell is shown in Fig. 6.

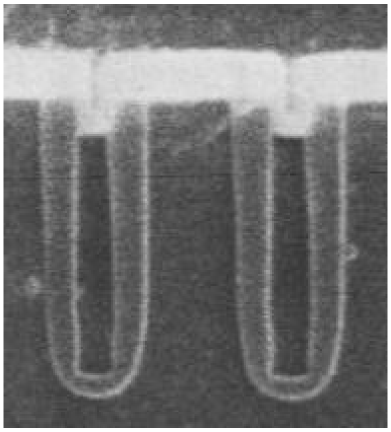


Fig 6. SEM cross section of the fabricated device

Breakdown and leakage sensitivity on trench depth is illustrated in Fig. 7.

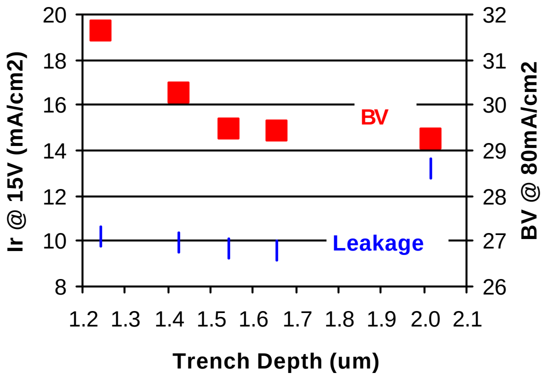


Fig 7. BV and leakage dependence on trench depth, measured from SEM cross-sections.

Thanks to the optimized Epi and trench design, Process tolerance analysis shows a wide process latitude for trench depth.

BV increases linearly by 7.2 V / um as trench depth is decreased from 1.55 to 1.25 um. This is in agreement with the simulation results. A slight decrease of BV and severe leakage increase for trench depth above 1.6 um can be explained by punch-through of the depletion region into the highly doped substrate region. A good margin with datasheet limits, 19mA/cm2 and 15V respectively for I_R and BV, is maintained over the entire range of trench depth considered.

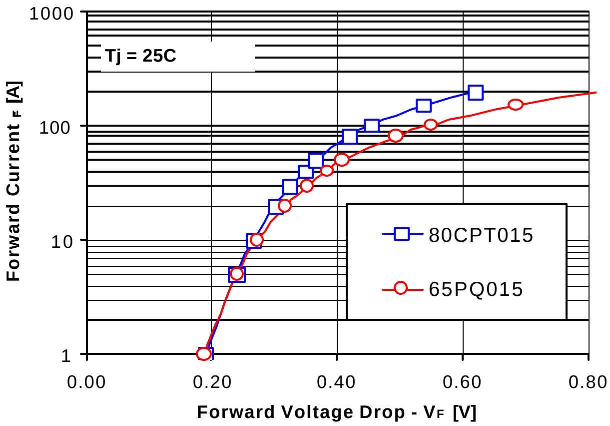
Each die is dimensioned to carry a 40A current with two assembled in a TO-247 package to create an 80A, common cathode, center tap device. Die top metal composition and thickness as well as the assembly process are optimized for a silicon trench structure. The new product was designated as 80CPT015.

IV. PARAMETRIC VERIFICATION

The main DC parameters are measured and compared against the International Rectifier Schottky "ORing" diode, 65PQ015. This planar device has same die area , bonding & assembly techniques and same TO247 package as the new part thus any comparison shown is truly related to the different Silicon technology.

1. Current-Voltage Characteristics:

I-V characteristics of the assembled devices are shown in Fig. 8. At 40A forward Current, 25C junction T, the trench device shows 36 mV lower Vf than the planar 65PQ015. The leakage at rated voltage is reduced by a factor 4. Similar improvement is observed at a higher junction temperature, allowing the trench device to be rated at $T_{j,max}$ =125 °C vs 100 °C for the planar device (at max reverse voltage).



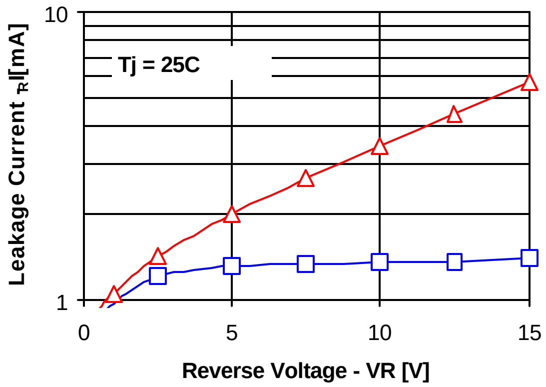


Fig 8. I-V characteristics of the assembled trench device 80CPT015 compared against the planar Schottky 65PQ015. Die size and assembly configuration are the same for the two devices.

2. Capacitance-Voltage & Switching Characteristics.

When the TMBS concept was initially presented, concerns were raised about the capacitance of the structure, where a MOS-like capacitor is formed in the trench electrodes effectively in parallel with the Schottky diode during operations.

In Fig.9 we compared the C-V characteristics of the new device with the conventional planar device by using a HP LCR meter.

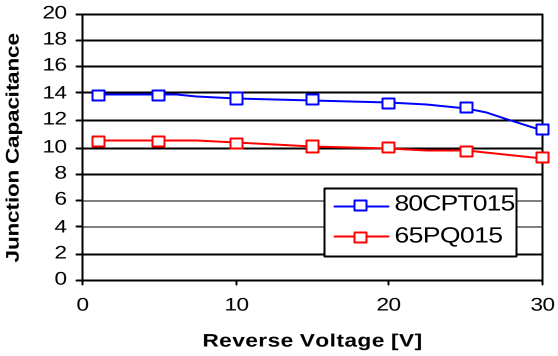


Fig 9. C-V Curve. Test signal frequency is 1 MHz.

At Vr=10V, the Trench capacitance is found to be 30% higher than the planar device with the same area. The increase compares with the severe 4x increase as observed in Ref. [1]. By an appropriate scaling of the oxide thickness To, the contribution of the gate oxide (C ~ 1/To) can be reduced dramatically.

Switching characteristics are comparable to planar device, as shown in Fig. 10.

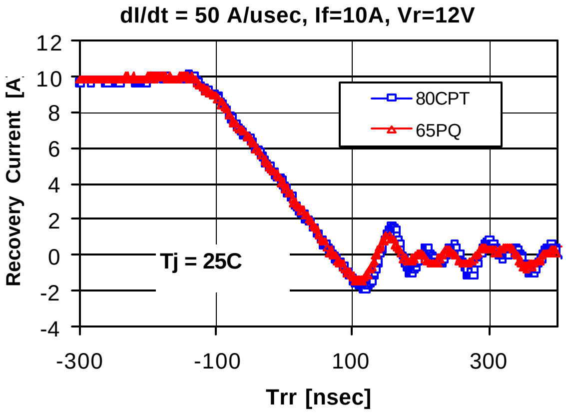


Fig 10. Switching characteristics

3. Eas – Reverse Avalanche Energy Characteristics

Reverse Avalanche conditions can be experienced by the Schottky Diode in “ORing” applications, were the device is used as a protections device, in the case of ESD during “Hot Swap”.

In SMPS applications where the Schottky is used as Output Rectifier, the device can experience a transient over-voltage in case of voltage spikes generated by the circuit. In both cases good avalanche absorption capability are required for the Schottky diode.

In Fig 11 we compare the Eas absorption capability over a wide range of load inductances.

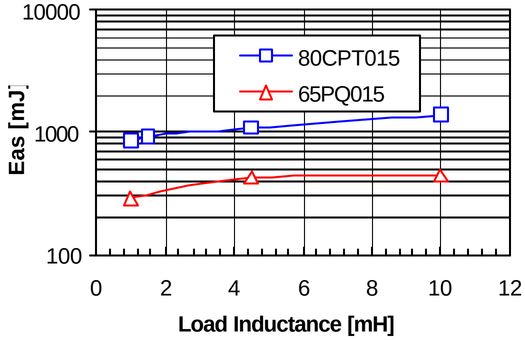


Fig 11. Avalanche test

The 80CPT015 is able to absorb twice the energy of the planar device before failure. This result can be explained by the different electric field distributions at breakdown, as observed during device simulations. Whilst in the conventional planar device E field crowding occurs in a limited region at the edge of the P+ guard ring, in the trench device the max E field is located near the trench bottom of each individual cell. Hence the whole active area is dissipating the avalanche energy, and the overall absorption capability is increased.

V. IN-CIRCUIT EVALUATION

In order to verify the benefit of the newly developed device, an in-circuit evaluation was performed in the OR-ing stage of a 750W commercial power supply. The module specifications are

- Input:100VAC-240VAC
- Output: 12VDC - 60A, 3.3VDC - 3A.

Only the higher voltage output is considered, no load is applied to the 3.3V Output.

Results are summarized in Fig 11, efficiency and device case temperature are monitored in 4 different configurations.

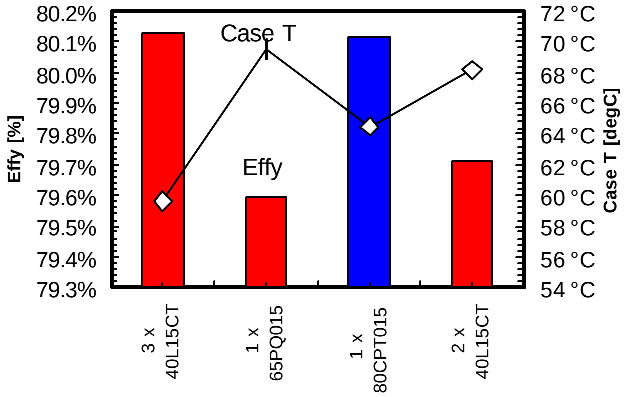


Fig 11: Efficiency test in an commercial unit were Schottky are used as “Oring” Diodes.

2x40L15CT devices are used in the basic configuration. 40L15CT is a 40A, 15V rated device, packaged in TO-220 with the same planar Silicon technology as the 65PQ015. First 2x40L15 are replaced by 3 devices of the same type: due to the increased conduction area and improved heat dissipation, the Forward Drop is reduced, 0.42 % efficiency increase and 8.6°C lower case temperature is observed. When the 3xTO220 are replaced by one 65PQ015 (TO247), efficiency dropped by 0.54 % and temperature increased by

10°C. Finally, one single Trench Schottky 80CPT015 is shown to achieve the same efficiency of 3xTO220s with a temperature increase of only 4.9°C. The single 80CPT015 solution utilizes 32% less Silicon than the 3xTO220 solution.

VI. CONCLUSIONS

A Trench MOS Barrier Schottky device has been developed and released into production by International Rectifier. To our knowledge, this is the first TMBS device in the Industry.

The optimization of trench depth and epi-thickness as key design features have been presented and the advantages of trench over planar technology reviewed, both as a single component and as a system solution.

The trench device offers 40 mV lower forward voltage drop and a reduction of a factor 4 in the leakage current compared to a benchmark planar device of the same voltage class and current rating.

Equivalent switching characteristics and a factor 2 higher reverse energy absorption capability are observed.

An efficiency test in a commercial unit is performed, with schottky used as protection devices in the “ORing” stage.

The benefits over planar technology as a system solution are summarized below:

- Increased efficiency for a single device solution
- Reduced component count, and improved current sharing.
- Improved reliability. $T_{j,max}$ is increased from 100 °C to 125 °C.
- Reduced footprint for the same efficiency.

References

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